ARPA QR6
PART B

LEVEL III

IMAGE TRANSMISSION VIA SPREAD SPECTRUM TECHNIQUES.

Part B.

ARPA Quarterly Technical Report. no. 6,
1 January 1976 – December 31, 1975.

Advanced Research Projects Agency
Order Number 2303
Code Number 3G10

ARPA Order-2343

264

1 January 1976
Naval Undersea Center
San Diego, California 92132

IMAGE TRANSMISSION
VIA
SPREAD SPECTRUM TECHNIQUES

Investigated by
DR. ROBERT W. MEANS (714:225-6872), Code 408
JEFFREY M. SPEISER (714:225-7621), Code 408
DR. EDWIN H. WRENCH (714-225-6871) Code 408
and
HARPER J. WHITEHOUSE (714:225-6315), Code 4002
Naval Undersea Center
San Diego, California

Sponsored by
Advanced Research Projects Agency
Order Number 2303
Code Number 3G10
Contract
effective: 15 February 1973
expiration: 30 June 1976
amount: $1,599,400

ARPA Quarterly Technical Report

January 1, 1975 – December 31, 1975

Form Approved Budget Bureau No. 22-R0293

FOREWORD

The enclosed reports have been submitted to the Naval Undersea Center by contractors who have been developing subsystems with applications to the Image Transmission via Spread Spectrum Techniques program. These reports make up Part B of ARPA QR 6–January 1976 quarterly technical report consisting of Parts A and B. For purposes of content identification these reports are numbered consecutively in Arabic numerals beginning with the title page of the first report and continuing to the end.

CONTENTS

CHARGE TRANSFER DEVICE DEVELOPMENT

by

D. D. Buss
W. H. Bailey
W. L. Eversole

Texas Instruments Incorporated

February 1975

Contract No. N00123-74-C-1366

Naval Undersea Center
San Diego, California 92132

TABLE OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS
(continued)

SECTION I

INTRODUCTION

The chirp z-transform (CZT) algorithm for performing spectral analysis is ideally suited to charge transfer technology because in the CZT, most of the computation is sampled-data convolution. The possibility of using charge transfer devices (CTDs) to implement the CZT was first discussed by Whitehouse, Speiser, and Means,[1] and the concept was first demonstrated by Means, Buss, and Whitehouse.[2]

The goal of Contract No. N00123-74-C-1366 was to develop CTDs suitable for taking the cosine transform of video images using the CZT. The objective is video bandwidth reduction by cosine transform encoding.[3]

CTDs fall into two categories: bucket brigade devices (BBDs) and the better-known charge coupled devices (CCDs). Of the two, CCDs can be operated at higher frequency and are the ultimate choice for the present video bandwidth reduction application. However, at the beginning of the contract a BBD filter design existed that could be quickly and cheaply recoded for the cosine transform application. Consequently, the program was divided into two parts: (1) an initial phase to produce 199-stage BBDs, and (2) a final phase to develop 63-stage CCD filters together with the electronics required to perform the cosine transform. Those two phases are discussed, respectively, in Sections II and III.

SECTION II

BUCKET BRIGADE DEVICE CHIRP Z-TRANSFORM

During the early stages of this contract, it was desired to obtain devices quickly so that the concepts of bandwidth reduction via the CZT could be demonstrated. A 200-stage BBD transversal filter had been developed previously at Texas Instruments under Contract No. F30602-73-C-0027, and this filter design could be quickly reprogrammed with weighting coefficients for the cosine transform. A detailed description of the design of this chip is given in the final report for that contract.[4] Key design features of this chip are summarized in Section II.A, and the test results on the ICs delivered to NUC in May 1974 under the current contract are summarized in Section II.B.

A. BBD IC Design

The BBDs were designed for low resistivity, n-type material ($\sim 1\ \Omega$-cm). The channel length was chosen to be L = 0.6 mil to give good charge transfer efficiency (CTE) at low frequency (below $f_c \approx 500$ kHz).

The cross section of the BBD is shown in Figure 1. The p-to-p spacing was 0.8 mil on the mask, resulting in an actual p-to-p spacing of 0.6 mil after diffusion. The overlap capacitance length was 0.8 mil, which assured good CTE up to 1 MHz. The charge transfer loss (1 - CTE) that can be expected from this design is shown as a function of frequency in Figure 2. In the lower resistivity material, the loss is smaller due to a smaller channel shortening effect.

The gate tapping technique was used to perform the weighted summation required to realize a transversal filter. This technique is described in Reference 5. The unit cell layout and circuit diagram are given in Figure 3. The magnitude of the weighting coefficient is determined by the length of the gate of T_L, and the sign is determined by whether the source of T_L is connected to Σ^+ or Σ^-.

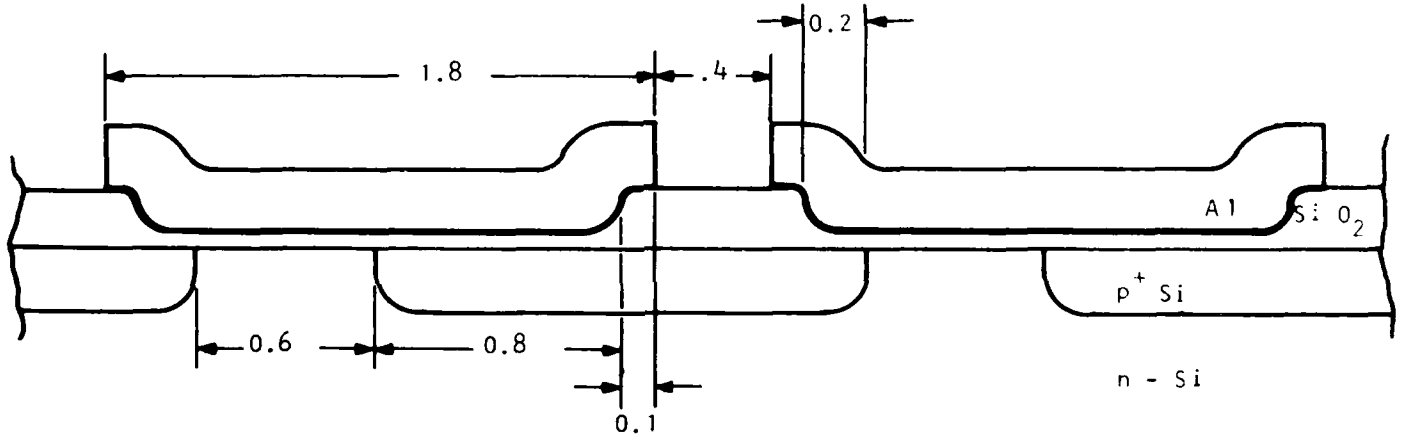


Figure 1 Cross Section of the BBD. The diffusion depth is approximately 0.1 mil, and the channel length is 0.8 mil on the photomask.

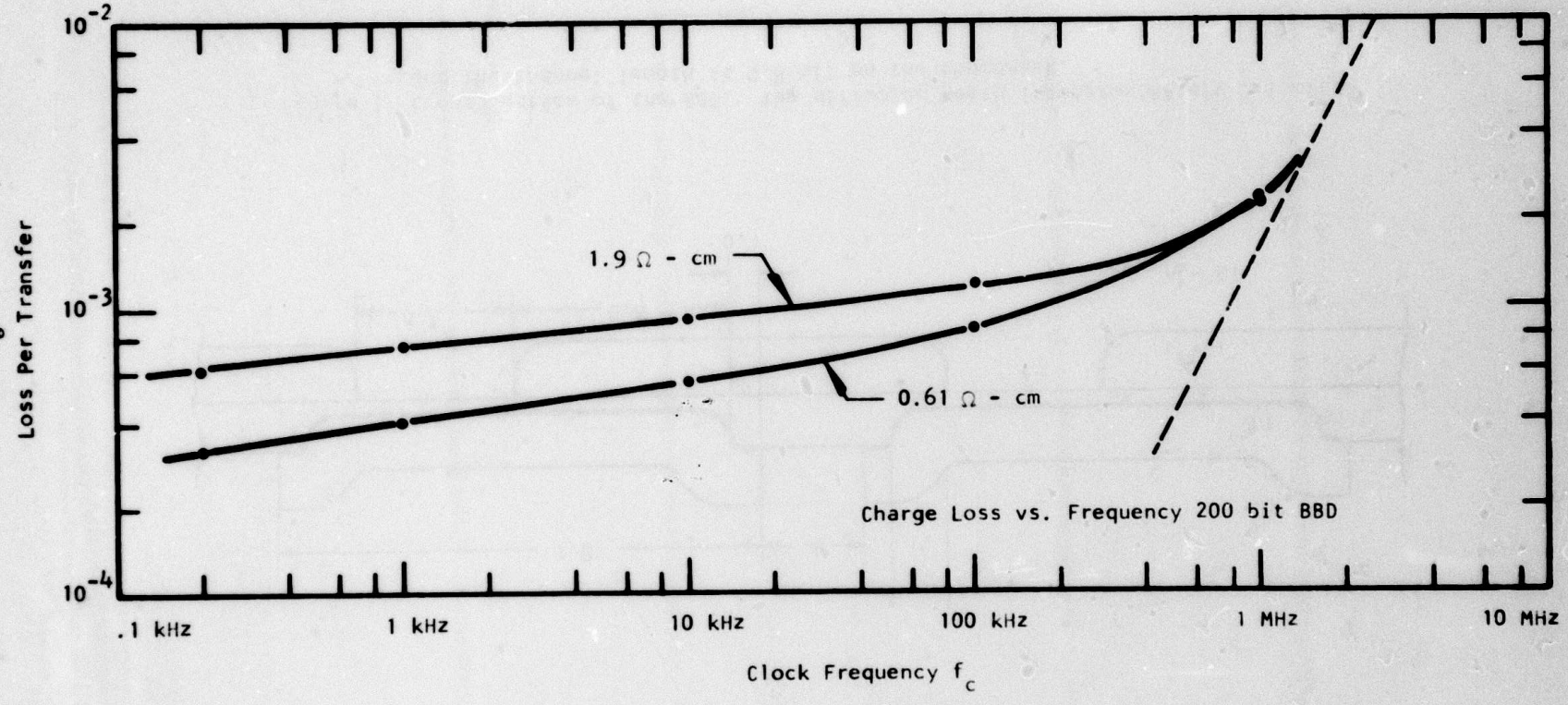


Figure 2 Charge Loss Per Transfer ε as a Function of Clock Frequency for 1.9 Ω-cm and 0.6 Ω-cm Devices. The dashed line corresponds to the calculated high frequency asymptote.

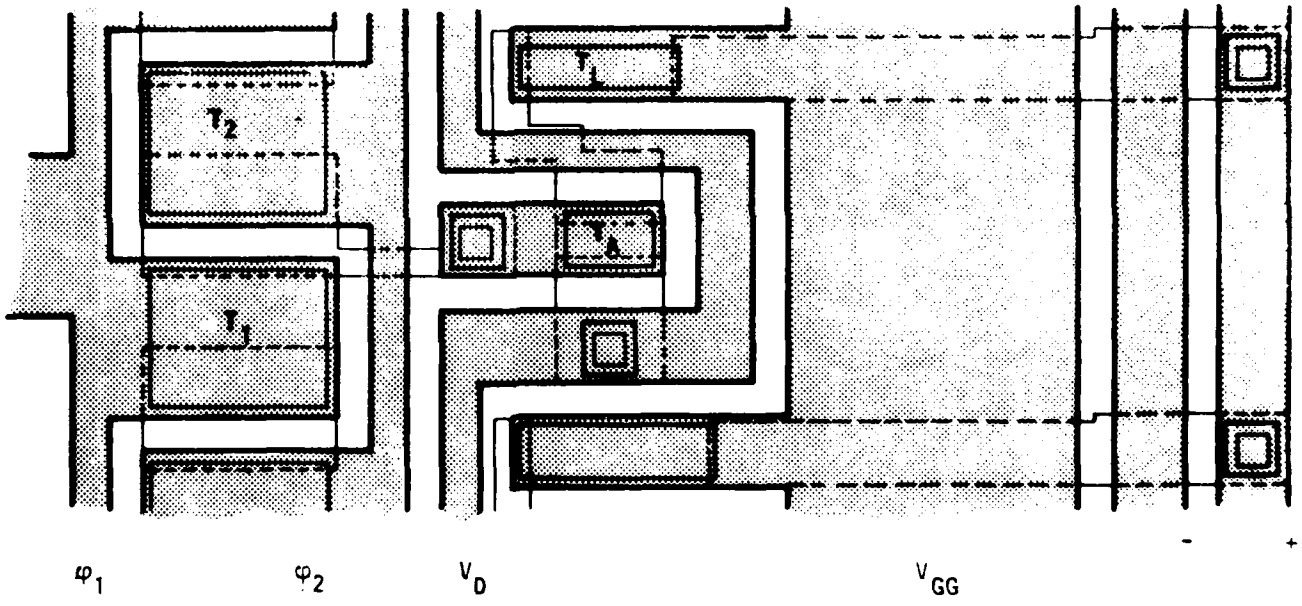


Figure 3(a) Layout of the Unit Cell. The circuit elements are labeled as in Figure 3(b).

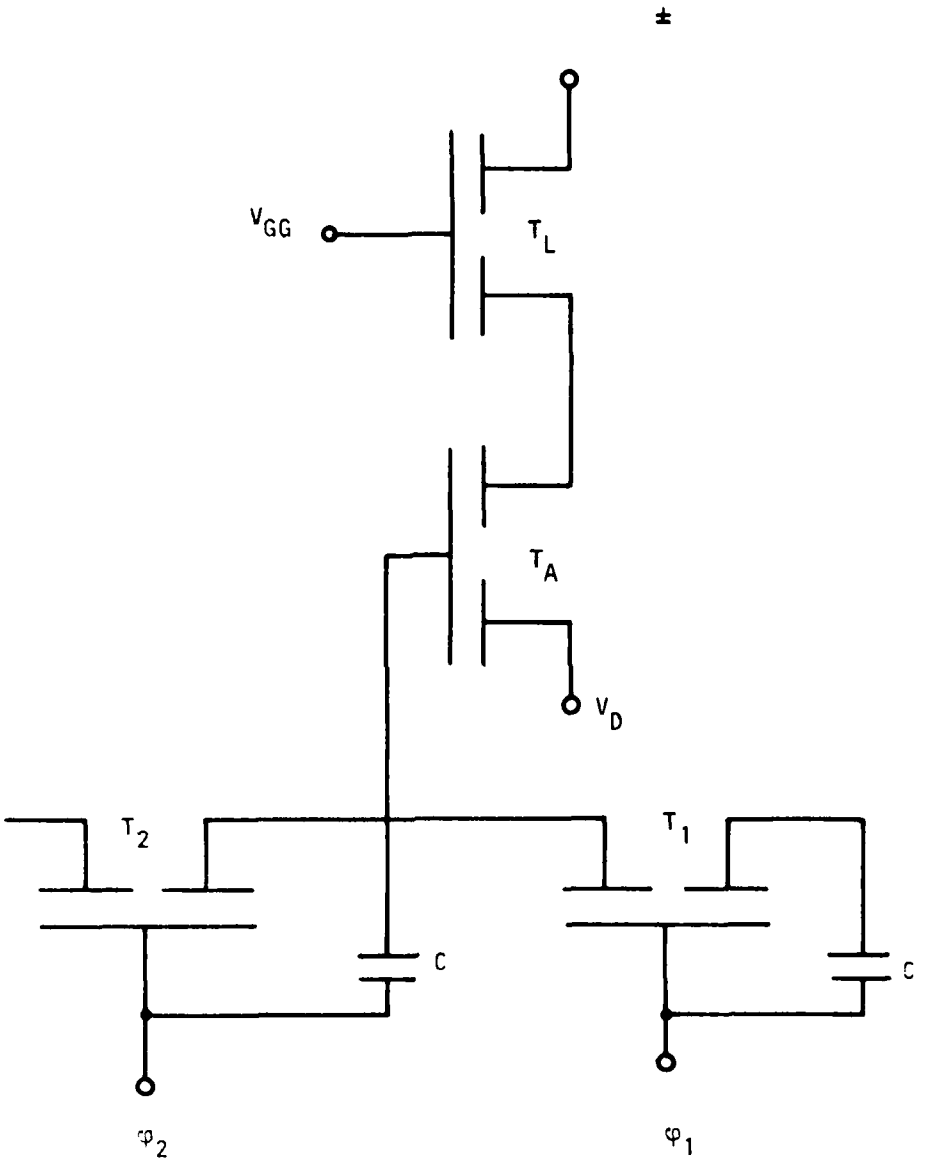


Figure 3(b) Circuit Diagram of the Unit Cell of Figure 3(a)

Because of the weighting circuitry, the BBD was laid out in a spiral fashion, as shown in Figure 4. The numbers of stages in each segment total 200. A photomicrograph of the chip is shown in Figure 5. Its overall dimension, including two filters, is 198 x 186 mil^2, and it is packaged in a 28-pin dual in-line ceramic package.

The input circuit was modified for the present application so that the filter output occurred during the time ϕ_1 was on (negative). The modified input is shown in Figure 6.

In order to perform a 100-point add cosine transform, 199 weighting coefficients are required. The two filters had weighting coefficients given by

$$h_k^{cos} = \cos\left[\frac{\pi(k-100)^2}{199}\right]$$

$$h_k^{sin} = \sin\left[\frac{\pi(k-100)^2}{199}\right] \qquad (1)$$

$$k = 1, 199.$$

Both filters are symmetric about the 100th tap. $h_{100}^{cos} = 1.0$ $\quad h_{100}^{sin} = 0.0$.

The BBD work performed under Contract No. N00123-74-C-1366 provides a good example of the usefulness of the factory-programmable filter concept. Aside from the modification of the input discussed above, (and this should not require modification in the future), the redesign for cosine transform application consisted of altering two photomasks to represent the modified weighting coefficients, and the reduction in the number of weighting coefficients from 200 to 199 was accomplished by making the last coefficient zero.

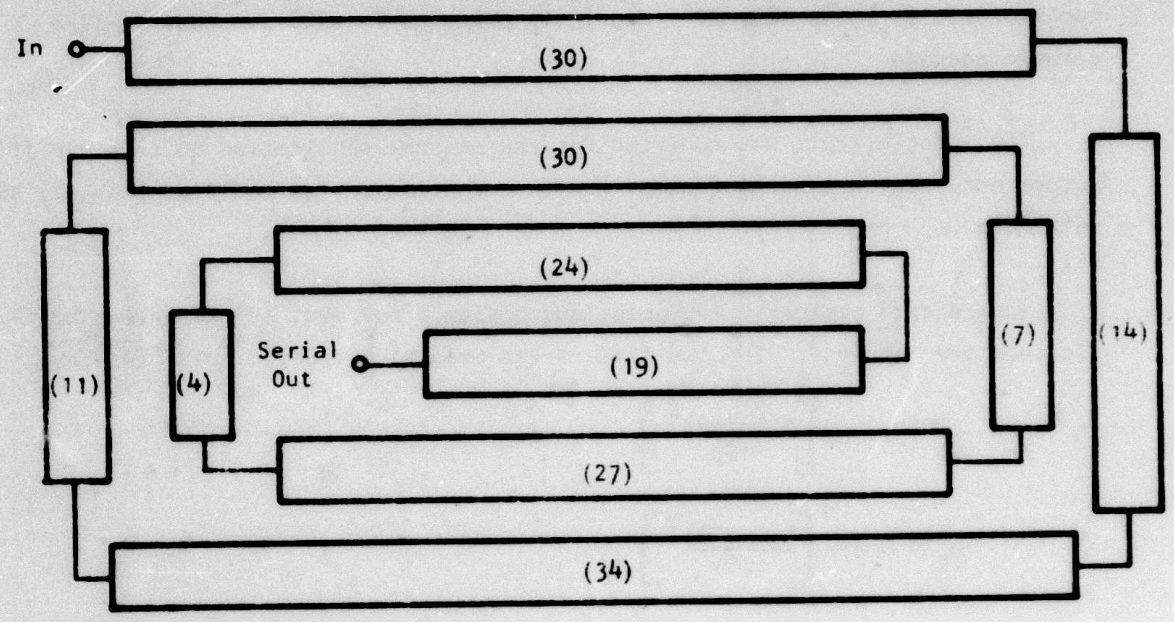


Figure 4 Schematic of the 200-Stage Filter

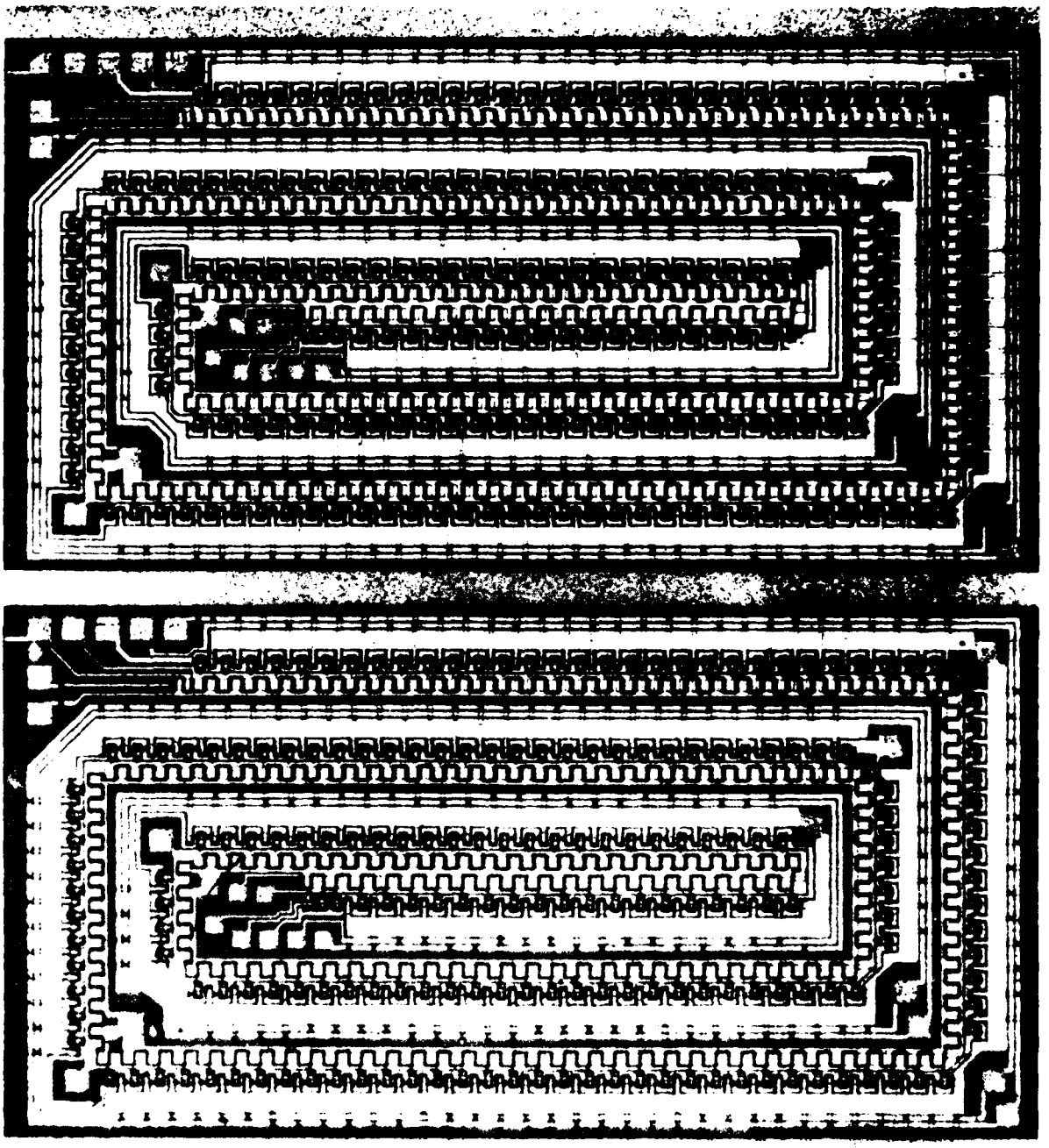


Figure 5 Photomicrograph of the IC Showing Both COS and SIN Filters

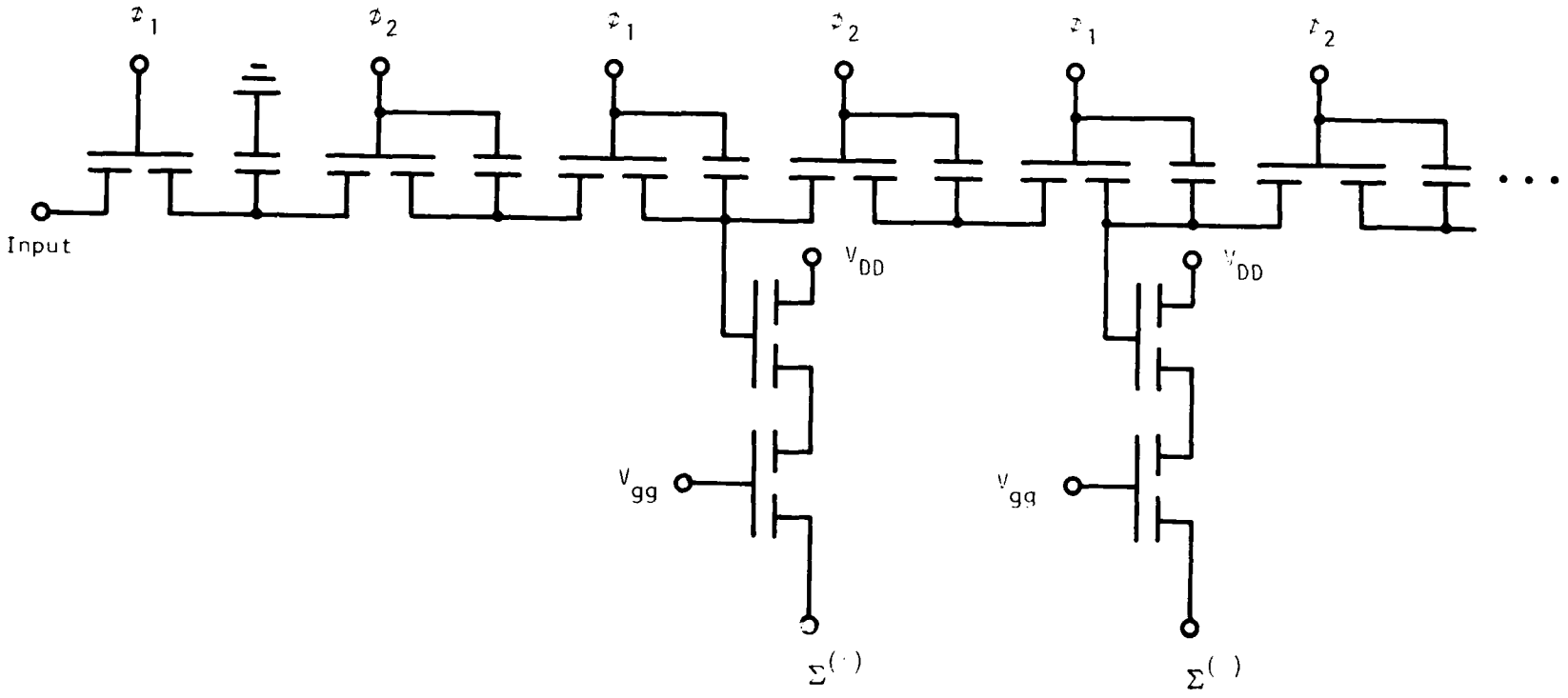


Figure 6 Circuit Diagram of the Input to the BBD Showing the First Two Coefficient Weighting Circuits

The cost and cycle time for this type of redesign can be extremely small, and it is anticipated that factory-programmed transversal filters will be an economical and versatile solution to a number of filtering problems.

B. BBD Characterization

One lot of 20 slices was processed. The material used was ⟨111⟩, phosphorus-doped, n-type, 0.55 - 0.85 Ω-cm; the process employed a composite oxide (500 Å), nitride (600 Å) gate insulator for low threshold voltage ($V_T \approx 1.5$ volt).

Ten dual 199-stage BBD filters were delivered to NUC on 22 May 1974. These devices were found to have CTE of 0.9993 when operated at 20 kHz with the following operating voltages:

V_{clock} = -12 V nonoverlapping pulses

V_{GG} = -20 V

V_{DD} = -20 V

$V_{substrate}$ = +5.2 V

$V_{input\ offset}$ = -4.4 V.

Figure 7 shows the device operating as a serial shift register, not as a filter. Twelve pulses are applied to the input, and the output shows rounding or step response error on the output. The fractional step response error given by $N\epsilon$ = (number of transfers) x (loss per transfer) ≈ 0.28, from which $\epsilon \approx 7 \times 10^{-4}$ is calculated. Reference to Figure 2 shows that $\epsilon \approx 7 \times 10^{-4}$ is quite consistent with previous results.

The responses of the two filters to a negative impulse are shown in Figure 8. The COS filter is shown at the top and the SIN filter is shown below. Attenuation of the amplitude of the impulse responses is apparent at the right of the photograph. This attenuation is due to imperfect CTE.

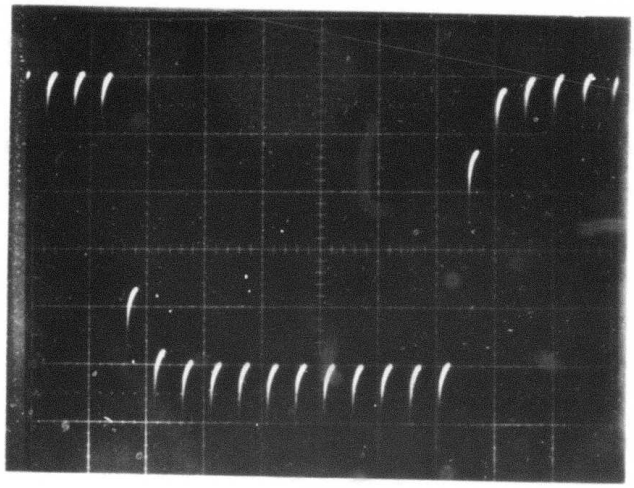


Figure 7 Serial Output of 200-Stage BBD

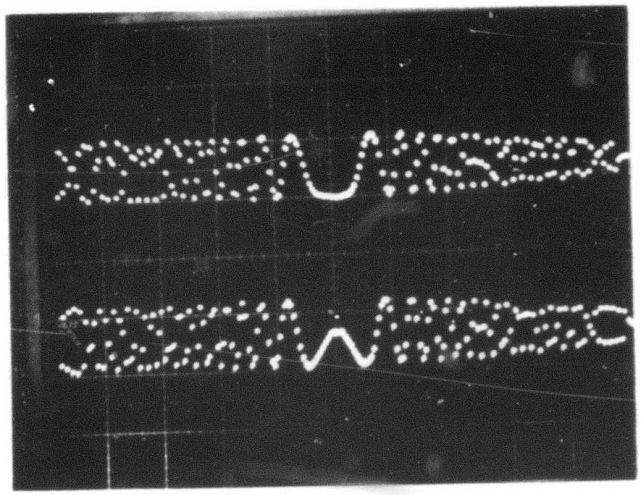


Figure 8 Typical Impulse Response of 200-Stage BBD

SECTION III

CHARGE COUPLED DEVICE CHIRP z-TRANSFORM

The goal of this phase of the contract was to develop a CCD chirp z-transform breadboard capable of operating at a 5 MHz clock rate. This breadboard performs the functions indicated in Figure 9 and is shown in detailed functional form in Figure 10. Involved in the development of this breadboard were the design and fabrication of a CCD filter bar, development of high speed differential current integrator (DCI) circuitry, development of high speed sample-and-hold circuitry, and evaluation and optimization of several analog multiplier circuits. Successfully interfacing these signal processing functions at the 5 MHz rate proved to be a difficult task.

A. Component Design

1. CCD Filter Bar

The metal mask for the filter bar designed under this contract is shown in Figure 11. The elements on the bar are identified by letters in Table I. The filters are four-phase, double-level, surface-channel devices with electrode weighting used on the ϕ_1 electrodes. The polysilicon-aluminum double-level metallization process was used to fabricate the devices. The CCDs have an electrode width of 6 mil and a length of 0.3 mil. The electrode weighting technique[5] has been used to perform the weighted summation required in a transversal filter. The filters are 63-stages in length with the first weighting coefficient occurring after the first stage. The input is shown schematically in Figure 12.

As shown in Figure 11, there are nine filters in all. Four of the filters are for the cosine transform (two COS filters and two SIN filters). These filters have weighting coefficients given by

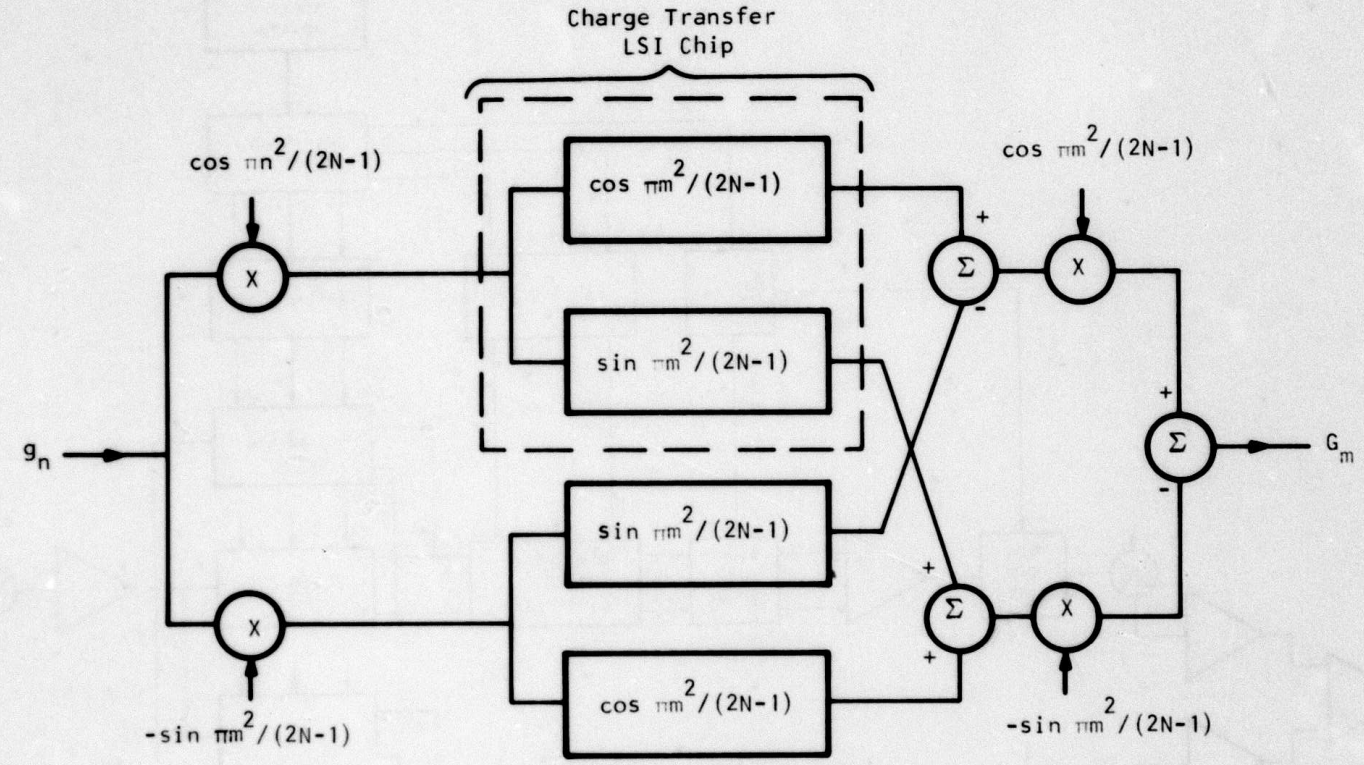


Figure 9 Mathematical Representation of CZT Algorithm

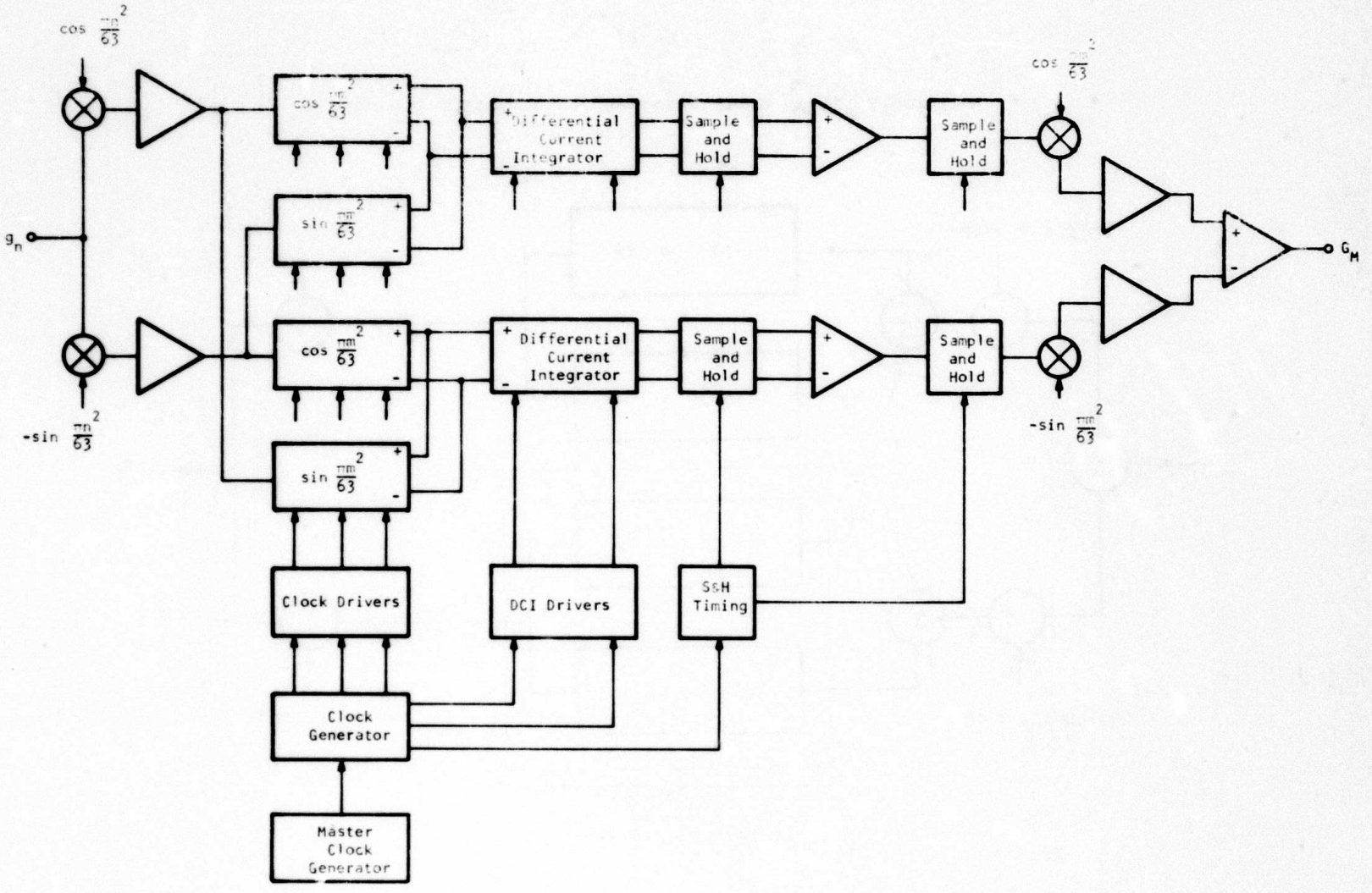


Figure 10 Functional Representation of CZT Breadboard

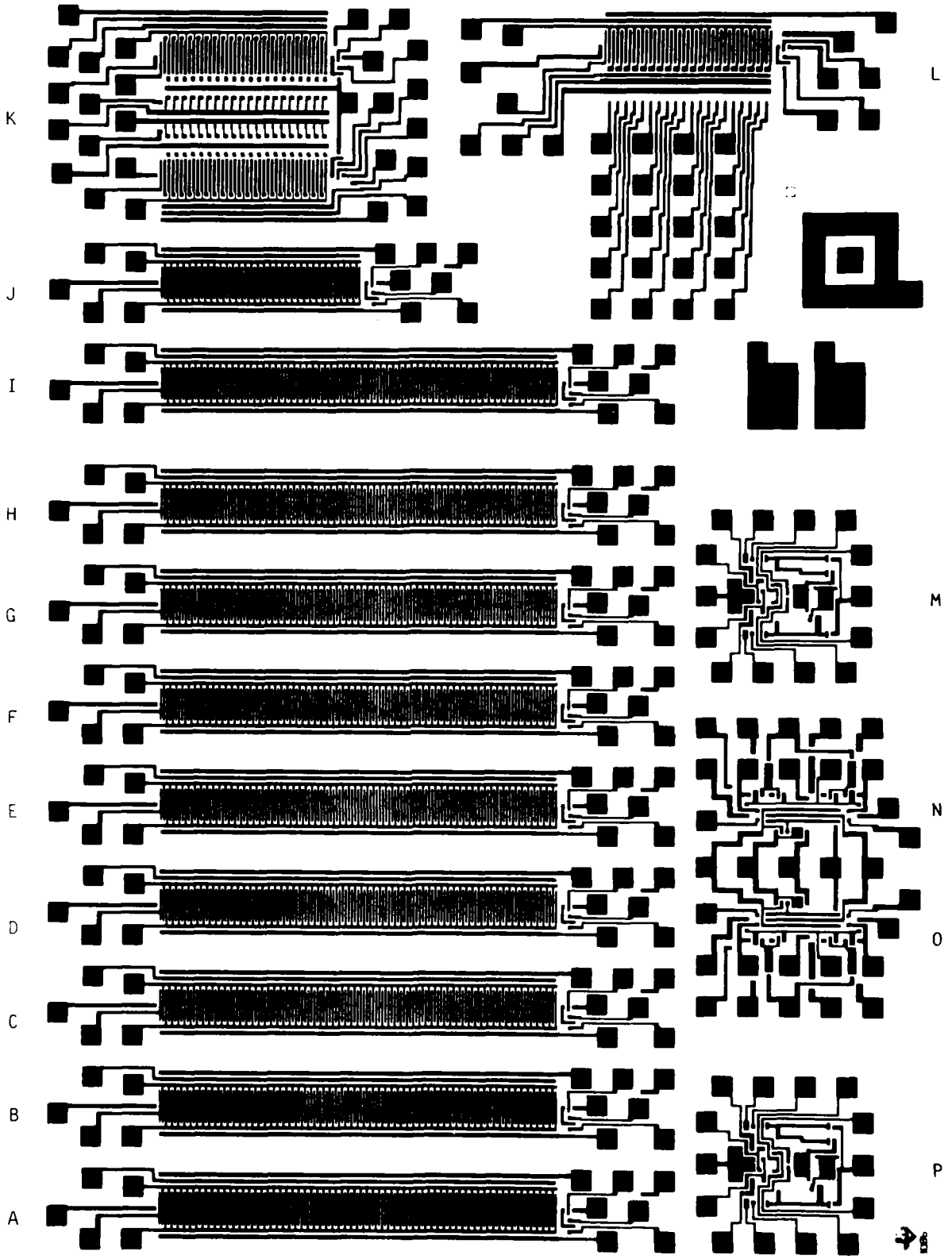
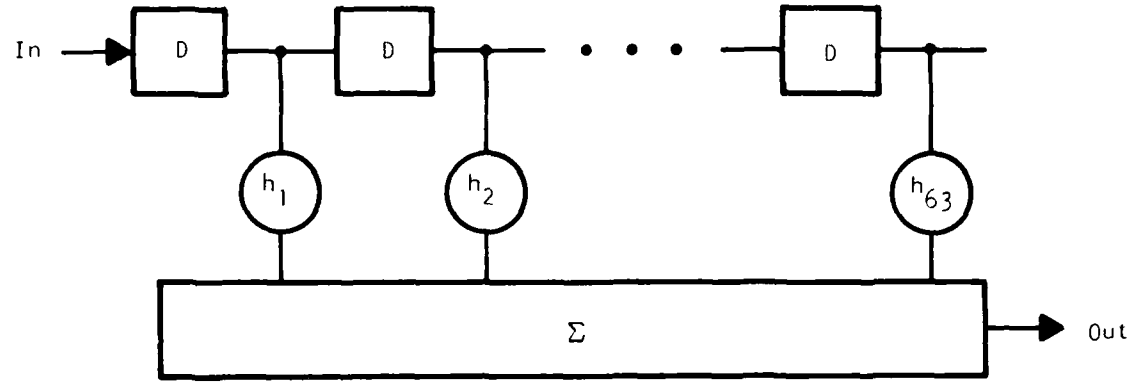


Figure 11 Metal Mask for the CCD Filter Bar. A scribe line (not shown) runs between filters H and I. The weighting coefficients appear on the poly mask.

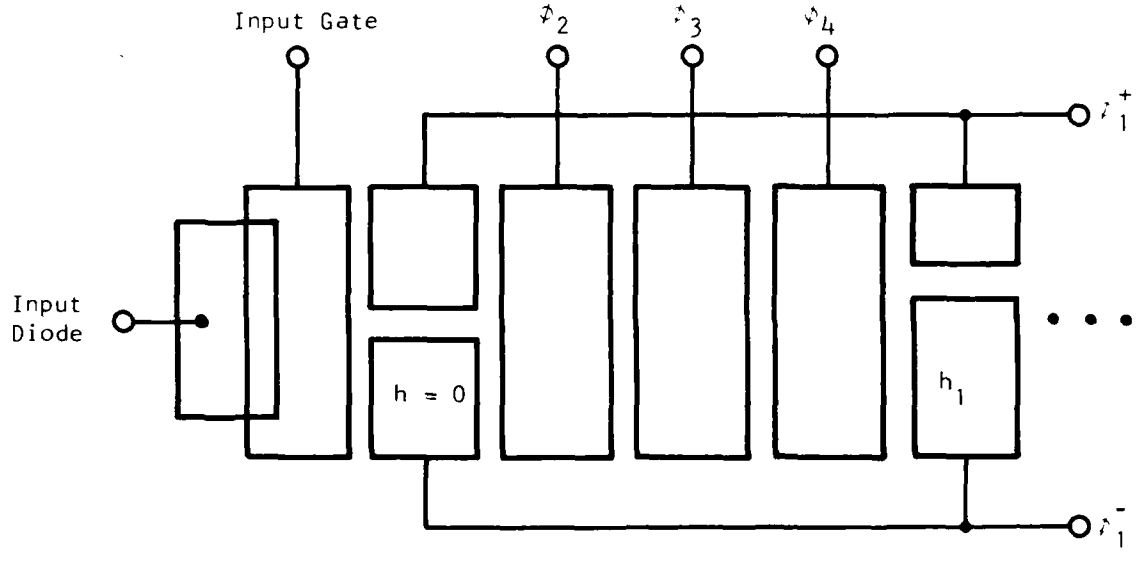
Table I

Contents of CCD Filter Bar

Reference Letter	Function	Length
B, D	Real Cosine Transform Filter	63 stages
A, C	Imaginary Cosine Transform Filter	63
F	Real Fourier Transform Filter	63
E	Imaginary Fourier Transform Filter	63
H	Real Apodized Cosine Transform Filter	63
G	Imaginary Apodized Cosine Transform Filter	63
I	Hilbert Transform Filter	63
J	Hilbert Transform Delay Line	32
N, O	Differential Current Integrators	-
M, P	MOS Analog Multiplier	-
L	Nondestructively Tapped Delay Line	20
K	Variable Tap Weight Convolution Filter	20
-	Process Evaluation Test Structures	-



(a)



(b)

Figure 12 (a) Schematic of the Transversal Filters Built Under This Contract. The input signal must be delayed by one clock period before it appears at the output weighted by h_1. (b) Schematic of the Electrode Layout on the CCD Input. The initial ϕ_1 electrode has zero weighting.

$$h_k^{COS} = COS\left[\frac{\pi(k-32)^2}{63}\right]$$

$$h_k^{SIN} = SIN\left[\frac{\pi(k-32)^2}{63}\right] \qquad (2)$$

$$k = 1, 63.$$

Two filters have Fourier transform weighting coefficients given by

$$h_k^{COS} = COS\left[\frac{\pi(k-32)^2}{32}\right]$$

$$h_k^{SIN} = SIN\left[\frac{\pi(k-32)^2}{32}\right] \qquad (3)$$

$$k = 1, 63.$$

Two filters were designed for the apodized cosine transform using Hamming weighting:

$$h_k^{COS} = W_k\ COS\left[\frac{\pi(k-32)^2}{63}\right]$$

$$h_k^{SIN} = W_k\ SIN\left[\frac{\pi(k-32)^2}{63}\right] \qquad (4)$$

$$k = 1, 63,$$

where $W_k = 0.544 + 0.456\ COS\left[\frac{\pi(k-32)}{31}\right]$, (5)

$$k = 1, 63.$$

The remaining filter was designed to implement a 32-point Hilbert transform. Its weighting coefficients are given by[6]

$$h_k = \begin{cases} A \left[\mathrm{COT}\left[\frac{\pi(k-32)}{63}\right] - \frac{(-1)^k}{\mathrm{SIN}\left[\frac{\pi(k-32)}{63}\right]} \right] & k \neq 0 \\ 0 & k = 0 \end{cases} \qquad (6)$$

$$k = 1, 63,$$

where A is a normalization factor. A 32-stage delay line was also designed to be used in conjunction with the Hilbert transform filter in applications such as single sideband generation.

In an effort to integrate as much as possible of the CZT electronics on a single chip, designs for an on-chip DCI and an MOS analog multiplier were included for evaluation. These designs proved incapable of 5 MHz operation, but do operate at lower frequency.

In addition to the above filters, two test structures were included that do not bear directly on the CZT application. Circuitry for nondestructively tapping a CCD delay line for an externally programmable transversal filter or for a time domain hydrophone beam-former were implemented in a 20-stage tapped delay line. These techniques were further extended to the construction of a 20-stage correlator that performs the convolution of two input waveforms. At the time of this writing, neither of these circuits has been tested.

The total bar size is 178 mils by 246 mils with an additional scribe line running horizontally between filter H and filter I of Figure 11. This scribe line is located so that the bar can be separated into smaller segments for ease in packaging.

2. Differential Current Integrator

The differential current integrator (DCI) is the output amplifier of the filter that integrates the transient clock current during the CCD's charge transfer process to perform the weighted summation required of the transversal filter. Figure 13 indicates the circuit implemented on the test bar. This circuit operates by precharging off-chip capacitors C_1 and C_2 that supply ϕ_1 clock pulses to the CCD while integrating the transient clock current. Transistors Q_1 and Q_2 are switches that charge capacitors C_1 and C_2 to V_{REF} when they are turned on by ϕ_3 pulses applied to the gates. When the ϕ_1 (complement of ϕ_3) pulse is applied to the gates of Q_3 and Q_4, they switch C_1 and C_2 into the ϕ_1^+ and ϕ_1^- clock lines. These capacitors supply the clock voltage pulses and integrate the transient clock current that flows as charge is transferred, producing a small voltage change across capacitors C_1 and C_2. Transistors Q_5 and Q_6 are pull-down transistors that pull the ϕ_1 clock lines to near ground when ϕ_3 is turned on. Transistors Q_7 and Q_8 form a source-follower with the source of Q_8 connected to the substrate in order to ensure that Q_5 and Q_6 can be completely turned off while ϕ_1 clock pulses are being applied to the CCD. Transistors Q_9 and Q_{10} are source-followers that form buffers between C_1 and C_2 and external amplifiers.

Transistors Q_{11} and Q_{12} are triple-gate MOSFETs that perform a sample-and-hold function. The first and third gates are on the lower interconnect level and are biased to a high dc level, while the second gate on the upper interconnect level is pulsed with a control pulse. This structure was designed to reduce the capacitive sample-and-hold pulse feedthrough by reducing the effective gate-to-source capacitance. Capacitors C_3 and C_4 are small storage capacitors, and transistors Q_{13} and Q_{14} are source-followers that buffer C_3 and C_4.

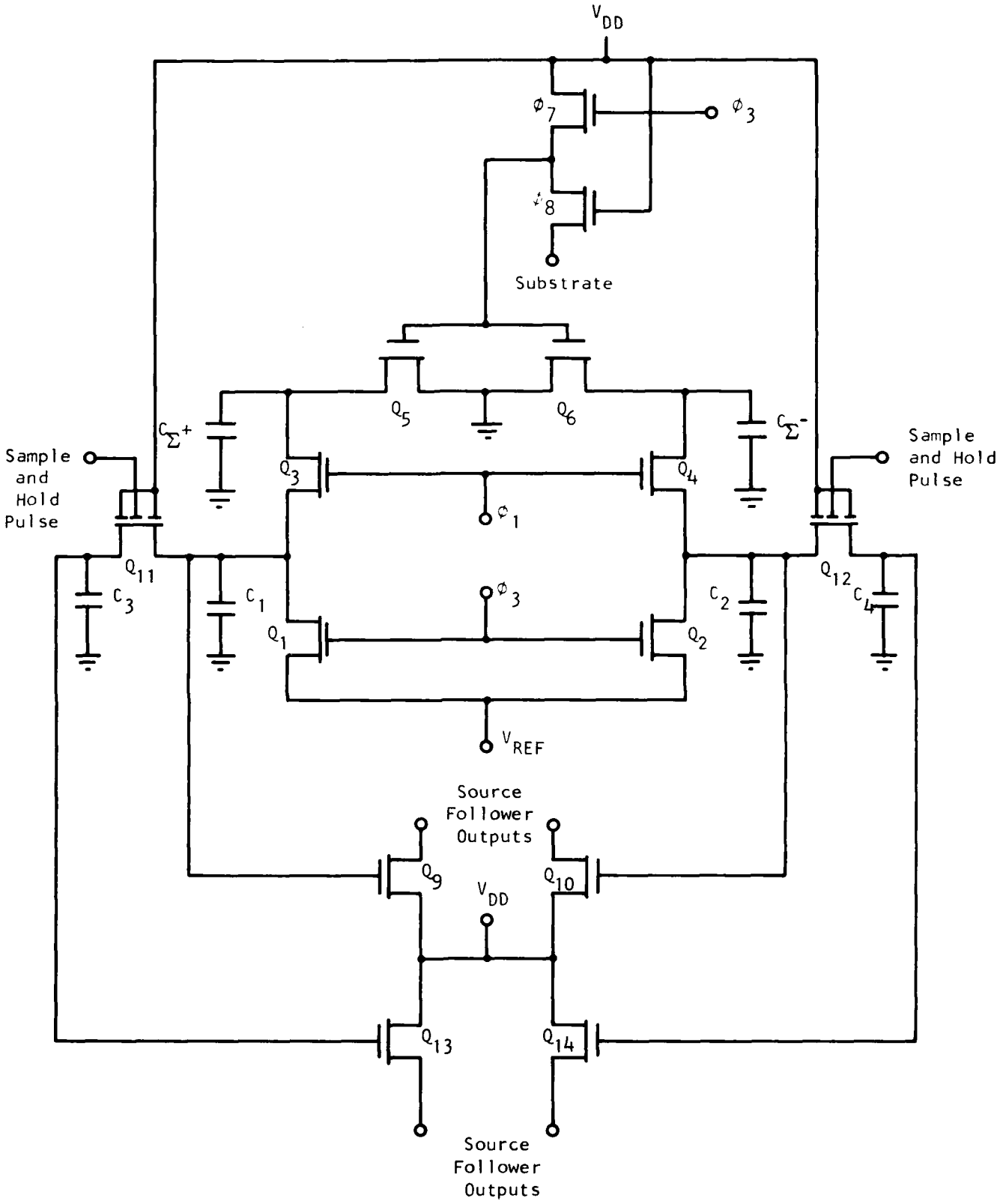


Figure 13 On-Chip Differential Current Integrator and Sample-and-Hold Circuitry

The on-chip DCI of Figure 13 was operable, but proved to be incapable of operation at the desired 5 MHz rate. Key problems are the long time constant associated with charging capacitors C_1 and C_2 through transistors Q_1 and Q_2 and poor operation of the triple-gate sampling transistors at high frequency. The failure of this DCI to operate at sufficiently high frequency was disappointing, but in analyzing its speed limitations, a new DCI design evolved which appears to be inherently faster. This improved DCI was realized in discrete component form in the breadboard, as discussed in Section II.B.4.

3. Analog Multiplier

The functional diagram of Figure 9 indicates the requirement for complex multiplications before and after the filter convolution operation. In analyzing existing designs for analog multipliers it became clear that these designs would not operate at the 5 MHz required by the system. For evaluation purposes, however, one of these designs was placed on the bar and was tested for linearity, dynamic range, etc.

This multiplier (shown schematically in Figure 14) functions in a manner similar to that of a conventional bipolar transconductance multiplier. Transistors Q_1 through Q_4 form a current source for the multiplier. Transistors Q_5 and Q_6 form two current paths that modulate the relative current amplitudes as a function of the differential X input voltage. Transistors Q_7 through Q_{10} again separate each of the two current paths into four current paths and modulate the relative current levels as a function of the differential Y input voltage. These four current paths are appropriately recombined into two paths which make their way through load devices Q_{11} and Q_{12} to the positive supply voltage. The differential ac voltage developed at the sources of Q_{11} and Q_{12} is proportional to the product of the X and Y differential input voltages. These nodes are buffered through source-follower transistors Q_{13} and Q_{14}.

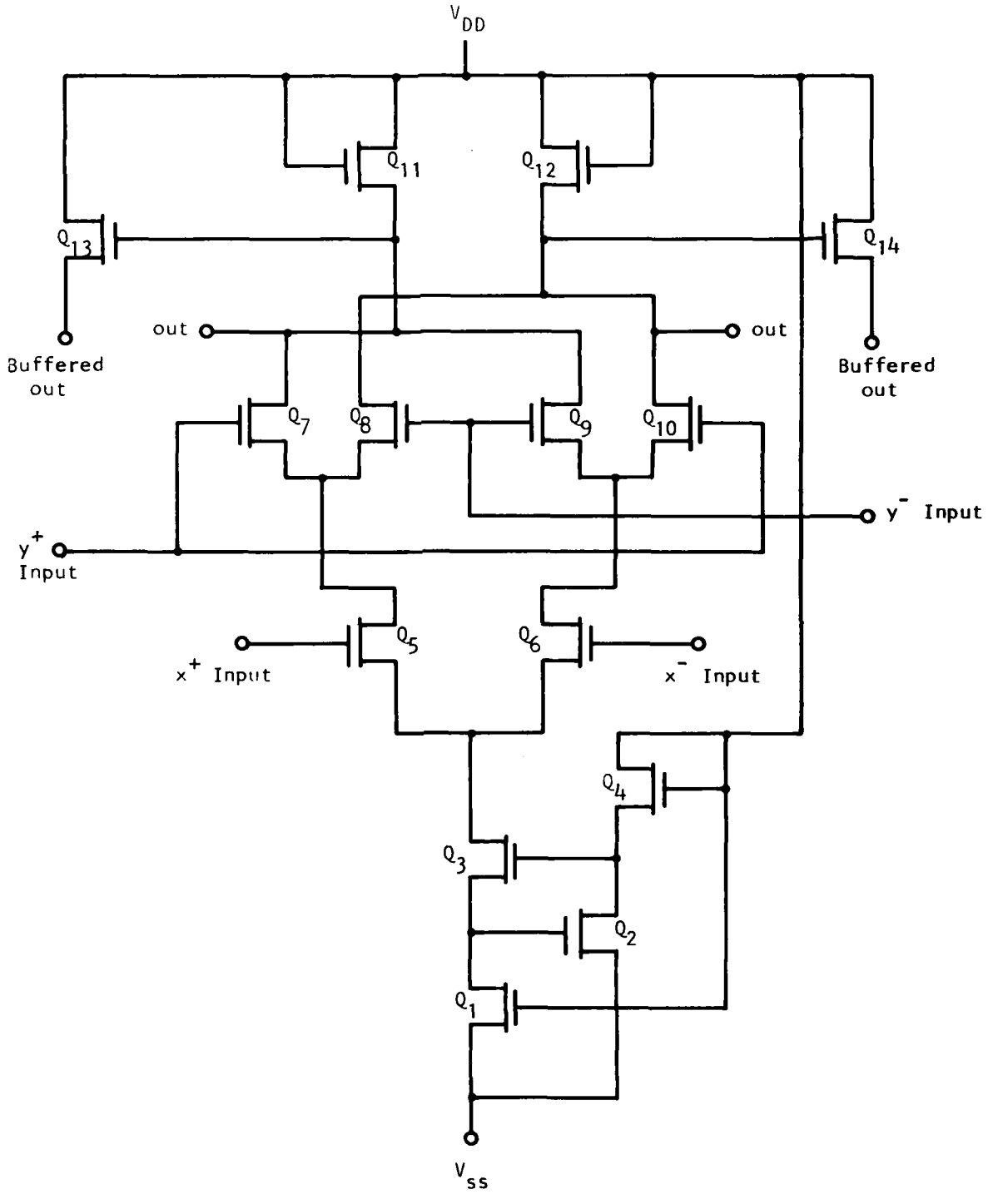


Figure 14 MOS Analog Multiplier Schematic Diagram

The results obtained with this multiplier are given in Section III.B.2. In the breadboard, however, off-chip bipolar multipliers were used to achieve the required 5 MHz.

B. Breadboard Development

Development of a CZT breadboard to implement the functional diagrams of Figures 9 and 10 at a 5 MHz data rate was one of the principal objectives of this contract. In addition to the CCD filters, Figure 10 indicates several other electronic functions: analog multiply, amplification, DCI and sample-and-hold clock driver, and chirp generation. The realization of these non-CCD functions occupied a major portion of the development effort. As a result of this effort the practicality of spectral analysis using CCD implementations of the CZT has been demonstrated, and a number of critical problems have been solved that should greatly improve future designs.

The completed breadboard for implementing the functions shown in Figure 10 is shown in Figure 15. The key electronic components in the breadboard are described in the remainder of this section.

1. CCD Filters

Nine CCD slices were processed using 10 to 20 Ω-cm, p-type, ⟨100⟩ material with a number of process variations. The lot history is summarized in Table II.

Seven of the nine slices were surface channel (SC) and two were buried channel (BC). Some of the buried channel devices were bonded, but to date these have not been evaluated. All the devices delivered under this contract were surface channel.

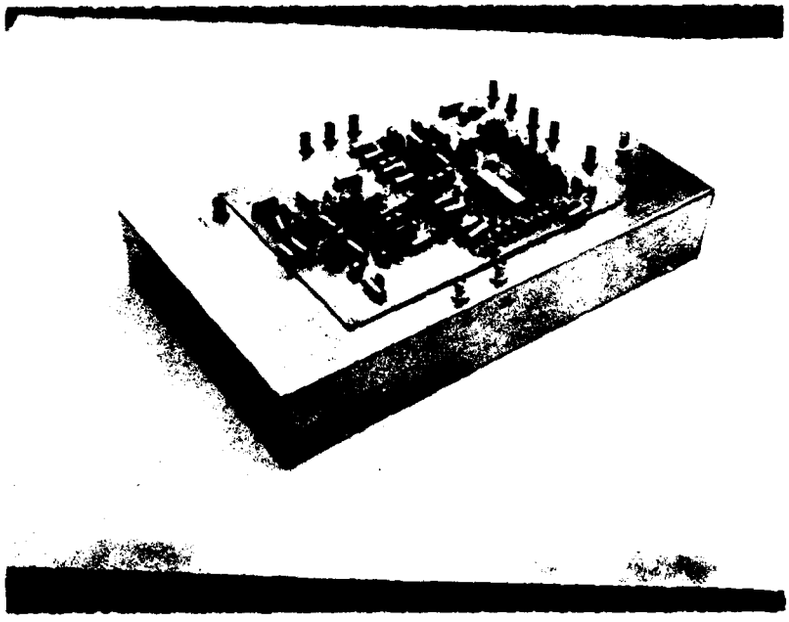


Figure 15 Chirp Z-Transform Breadboard

Table II

Lot History for CCD Filter Bar

Slice No.	SC*/ BC†	Oxide Thickness (Å)	Metallization	Dc Probe Yield (%)	No Ink	Number Bonded	Good Devices
1	SC	1500	poly/Aℓ	not probed -- used for photographs			
2	SC	1500	poly/Aℓ	77	18	19	10
3	SC	1500	poly/Aℓ	81	23	22	13
4	SC	1500	poly/Aℓ	68		7	4
5	SC	1500	poly/Aℓ	79			
6	BC	1500	poly/Aℓ	80	10	6	not tested
7	SC	2000	poly/Aℓ	80			
8	SC	2000	double poly	low			
9	BC	2000	double poly	zero			

* Surface channel

† Buried channel

Seven of the slices used the conventional poly/Aℓ metallization in which the first interconnection level is poly-Si and the second level is evaporated Aℓ. Two of the slices were processed using two levels of poly. A diode contact problem made the dc probe yield on these devices low, but several of these surface channel devices worked very well. All the devices delivered utilized the poly/Aℓ metallization.

At the time these devices were processed, only dc testing could be performed on the automatic testers. Such testers check for opens and shorts in the clock lines, input, output, etc. Eight filters on each bar were tested, and those that failed dc test were inked. The fraction of filters that passed dc probe test is given by slice in the column marked "dc probe yield." On approximately 50% of the bars, all four cosine filters were good.

Several bars from slices 2, 3, 4, and 6 were bonded. The bars selected for bonding were mostly those having no ink (all good filters). The bonded devices were tested by checking their serial operation in a working test box at 1 MHz. If devices required adjustment of operating voltage levels, they were rejected. The 20 best devices were selected for delivery.

Figure 16 shows part of the impulse response of a COS and a SIN filter compared with the chirp as generated from the PROM chirp generator (see Section II.B.6). The photo shows the later half of the impulse responses where the effects of charge transfer loss are greatest. The postmultiply chirp waveform is displaced one bit to the left from the impulse response.

The filter responses are inverted because a negative impulse is applied. The chirp waveforms are inverted on the scope. Figure 16 also shows the calculated impulse responses for four-point cosine transform filters.

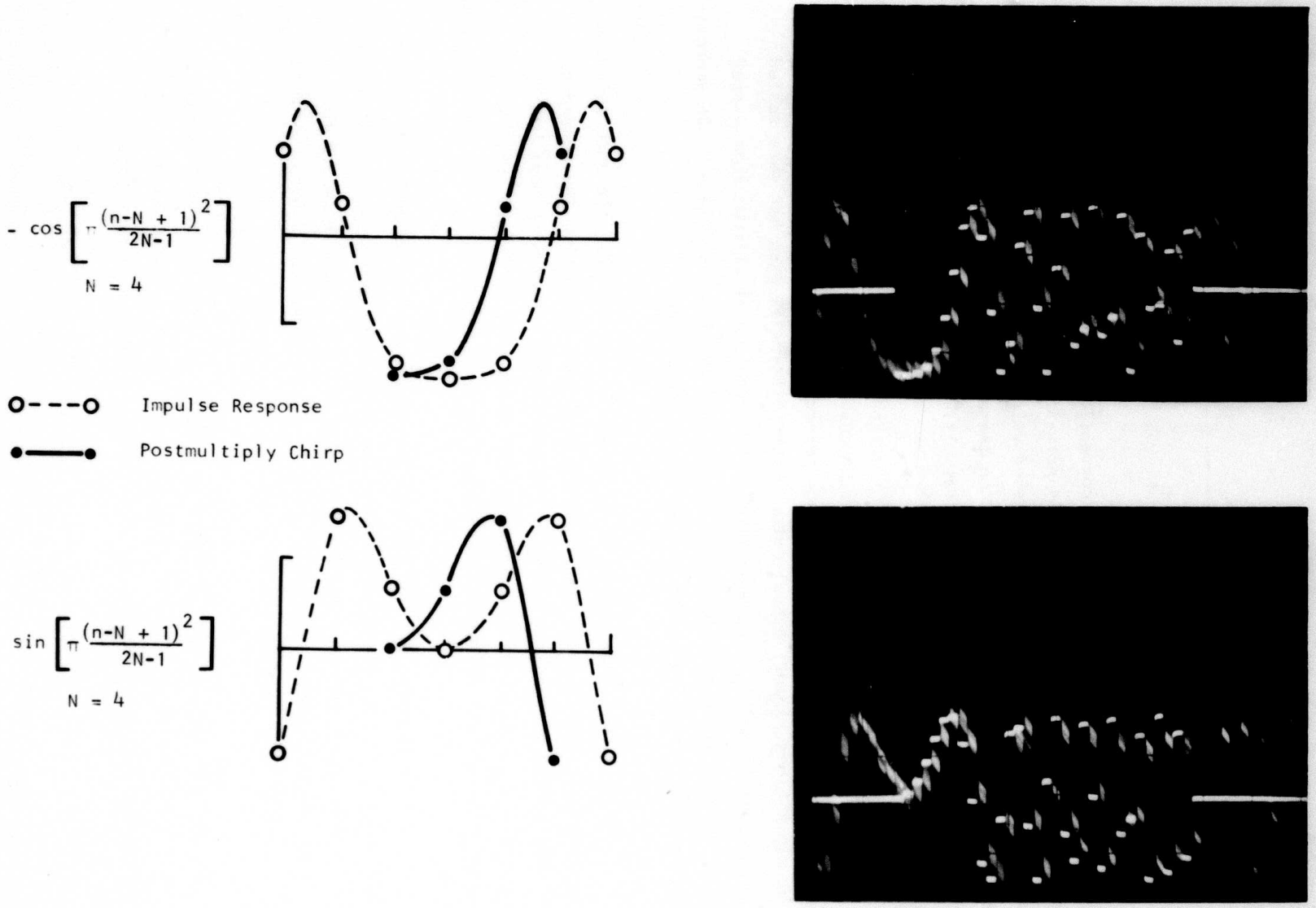


Figure 16 Impulse Response of the COS (Top Right) and SIN (Bottom Right) Filters. Only the latter half is shown, and it is compared with the postmultiply chirp displaced one bit to the left. A drawing is shown at the left of the equivalent impulse responses and postmultiply chirps for an N = 4 system.

The operating voltages that optimize filter operation are given in Table III.

Table III

Dc Operating Voltage Ranges for CCD Filters

Input Diode	2.5 to 6 volts
Input Gate	10 to 12 volts
Output Gate	3.5 to 6 volts
V_{DD}	10 to 15 volts
Substrate	-2.5 to -4 volts
Clock Pulses	10 to 15 volts

When the CCDs were operated in the tester with optimized clocks, the CTE was normal for devices of this design: 0.9998 at low frequency, as shown in Figure 17. However, when the CCD was operated in the breadboard, the CTE was degraded somewhat. Loss per transfer measured while operating in the breadboard is shown in Figure 18 as a function of frequency. The results indicate a low frequency CTE of 0.9996, decreasing to 0.9991 at 5 MHz. This could be improved somewhat by optimizing the clocking waveforms in the breadboard.

2. Analog Multiplier

Experimental evaluation of the multipliers of Figure 14 indicates the current source is sensitive to MOSFET threshold voltage variations. Several slices have shown operation with transistors Q_5 through Q_{10} saturated (i.e., $V_{DS} \approx 0$) due to high currents (approximately three times the design value). These slices showed slightly positive threshold voltages due to process improvements. Other slices having negative threshold voltages near the design value were

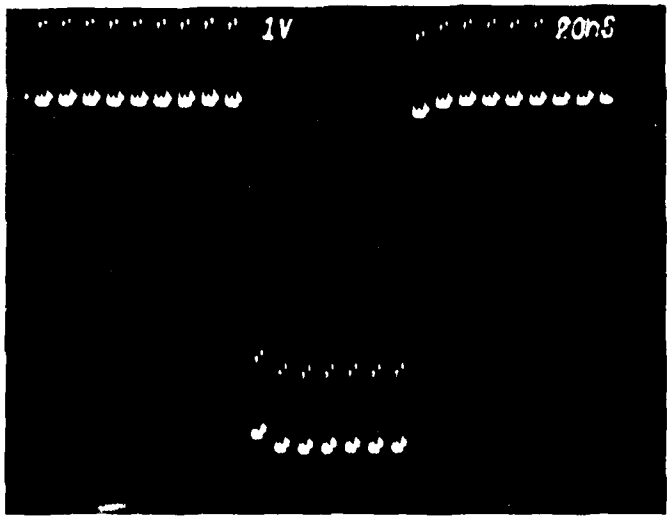


Figure 17 Serial Output of the CCD Filters Operating in Tester with 15 Volt Clocks. At f_c = 250 kHz. CTE = 0.9998.

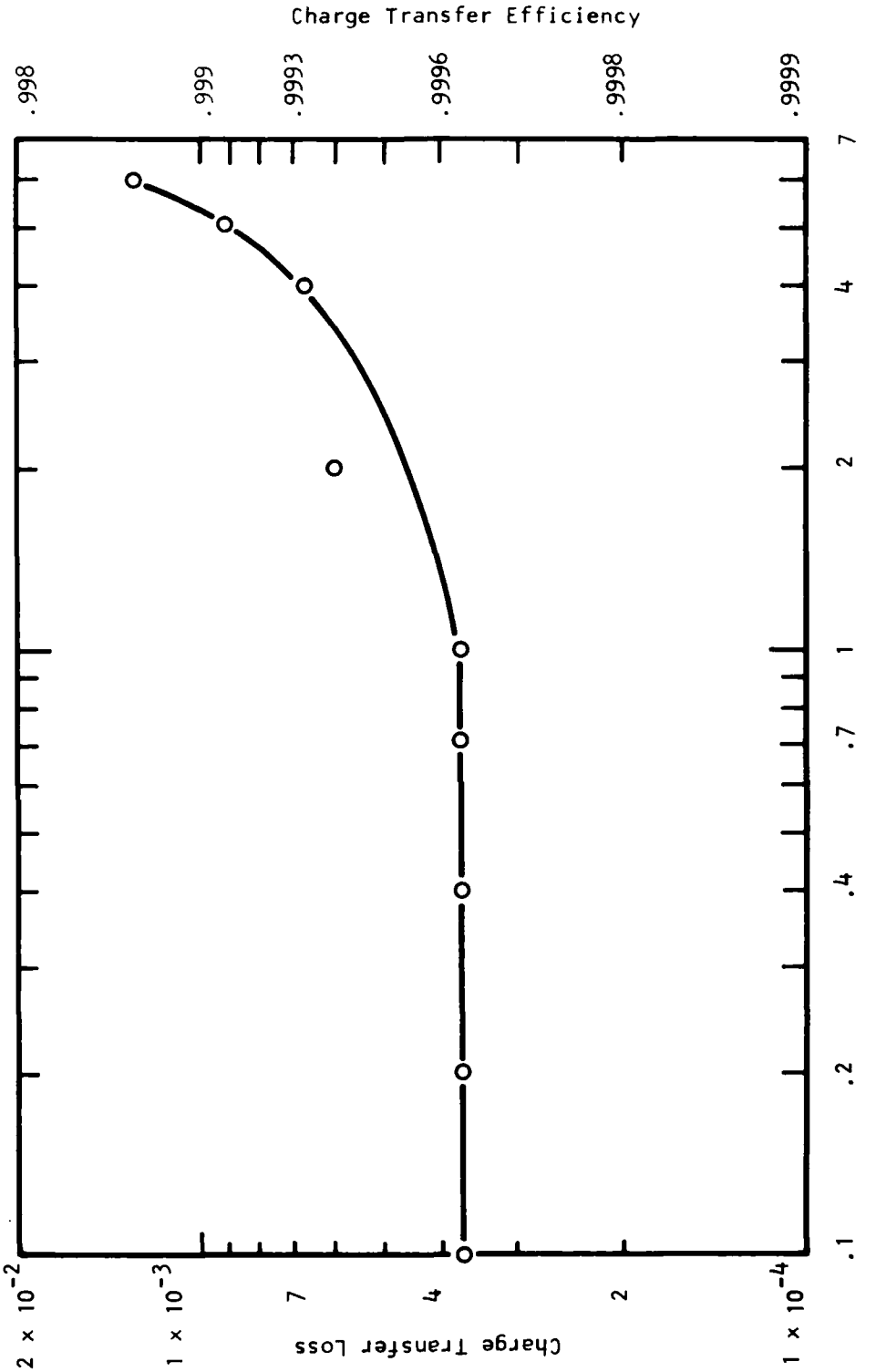


Figure 18 Charge Transfer Characteristics vs Clock Frequency for CZT Breadboard (10 Volt Clock Pulses)

found to be functional and performed much as expected from computer simulation. Figure 19 indicates operation of this multiplier when used to perform a squaring function. Figure 20 qualitatively demonstrates operation of the chip.

In order to operate over an input signal bandwidth compatible with a 5 MHz clock rate, other multipliers were evaluated. Analog Devices Model AD429 hybrid multiplier and Model AD530 monolithic multipliers and Motorola MC1595 monolithic multipliers have been evaluated at TI. Very little difference in high frequency characteristics could be detected between a properly adjusted MC1595 and the AD429, primarily due to the dominance of high frequency feedthrough. The AD429 is simpler to operate and adjust, but lower cost and slightly more flexibility of the MC1595 made it more attractive for use in this breadboard.

Attempts to null the inputs of the MC1595 indicated the Y input feedthrough could not be nulled as well as the X input. As a result, the chirp signals were applied to the X input to reduce the zero frequency correlation peak resulting from the feedthrough of the chirp waveform. It is believed that high frequency performance of this multiplier is limited by the high frequency characteristics of the transistors utilized in the IC design. Attempts to improve high frequency feedthrough characteristics by using an external current source constructed of high f_T devices produced no significant improvement. Imperfect device matching, insufficient high frequency properties of transistors, and excessive parasitic capacitance are believed to be the causes of the less than desirable performance of these multipliers. This conclusion is partially confirmed by Gilbert.[7]

Optimal nulling of the MC1595 multipliers and optimization of the remaining circuit components have given acceptable multiplier operation over the desired bandwidth. The feedthrough problem might be a severe limitation of the present system for very precise or wide dynamic range spectral analysis.

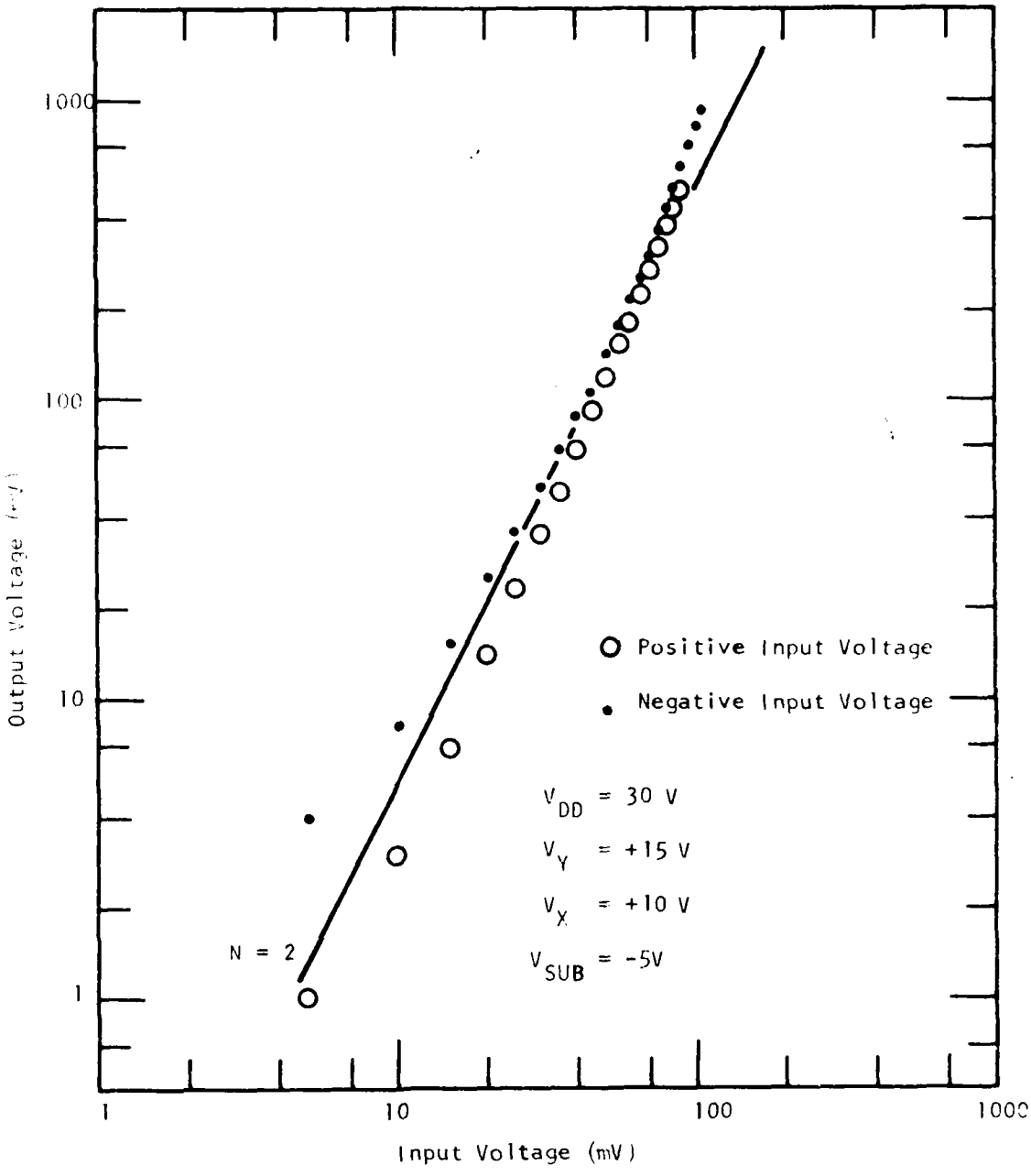


Figure 19 Dc Squaring Characteristics of MOS Analog Multiplier

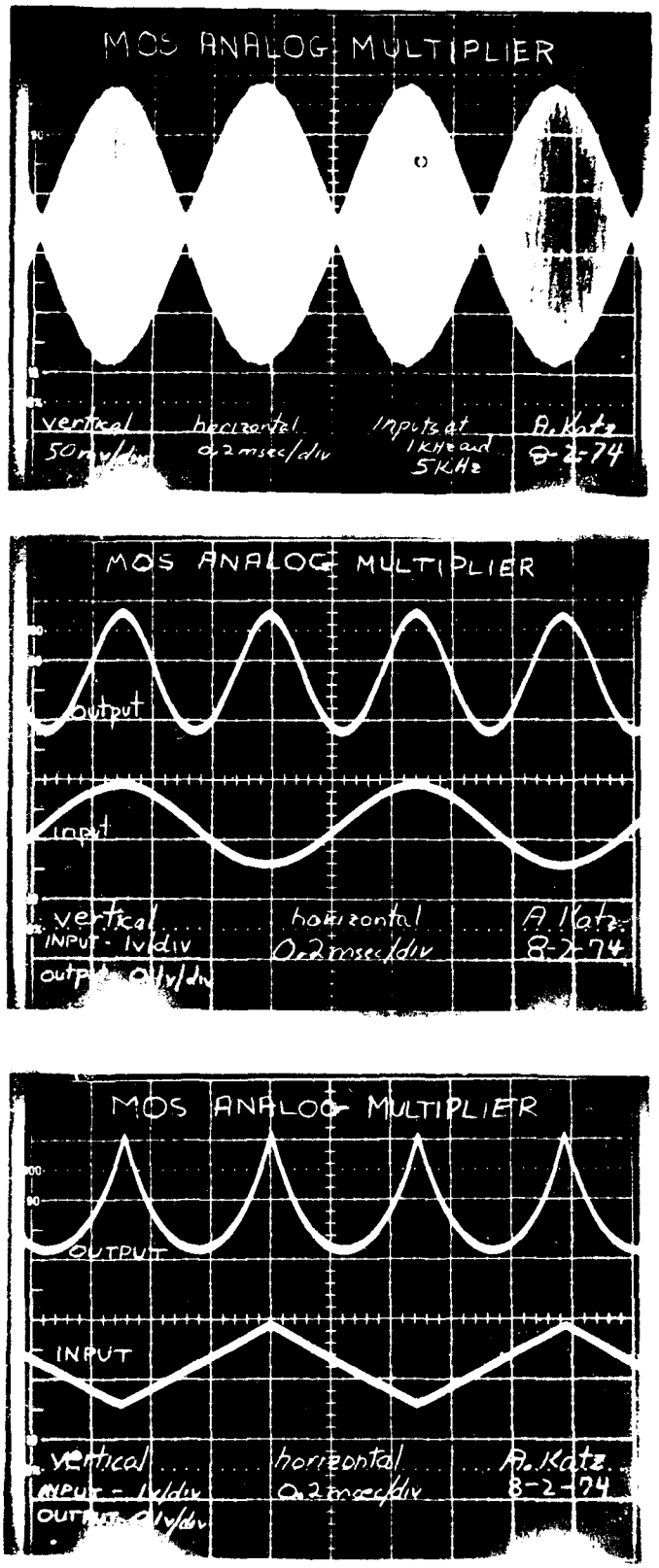


Figure 20 MOS Analog Multiplier Operation. (a) two sinusoids, (b) a single sinusoid applied to both inputs, and (c) a sawtooth applied to both inputs.

3. Amplifiers

The necessity to achieve flat gains over a 5 to 10 MHz frequency range was a very stringent requirement that most monolithic operational amplifiers were unable to meet. The SN7511 and SN72733 video amplifier ICs appeared to have sufficient bandwidth for this application. The difficulty in using feedback and the peaked high frequency response that accentuates ringing of the SN72733 made it less attractive than the SN7511. The primary disadvantage of the SN7511 was the requirement for different compensation networks with different closed loop gains. Potential oscillation problems due to improper layout were experienced at times, but are characteristic of any broadband amplifier. Figure 21 indicates the gain characteristics of the SN7511 utilized in the breadboard.

4. DCI and Sample-and-Hold Circuitry

The on-chip DCI of Figure 13 operated at low frequency, but failed to operate at the design goal of 5 MHz. Key problems were the long time constant associated with charging capacitors C_1 and C_2 and poor operation of the triple-gate sampling transistors at high frequencies.

In the final breadboard, the DCI was composed of discrete components, and a fundamental design change was found to improve speed. In the DCI design of Figure 13, capacitors C_1 and C_2 are charged to the clock voltage, and then these capacitors are used to charge the clock line capacitances C_{Σ}^{+} and C_{Σ}^{-}. In the new design shown in Figure 22, the clock line capacitances C_{Σ}^{+} and C_{Σ}^{-} are charged with C_1 and C_2 in series. This circuit operates well at 5 MHz in discrete component form and could be integrated in IC form more readily than the design of Figure 13.

The operation of the DCI of Figure 22 is as follows. The ϕ_1 clock pulses are applied to the weighted ϕ_1 filter electrodes through capacitors

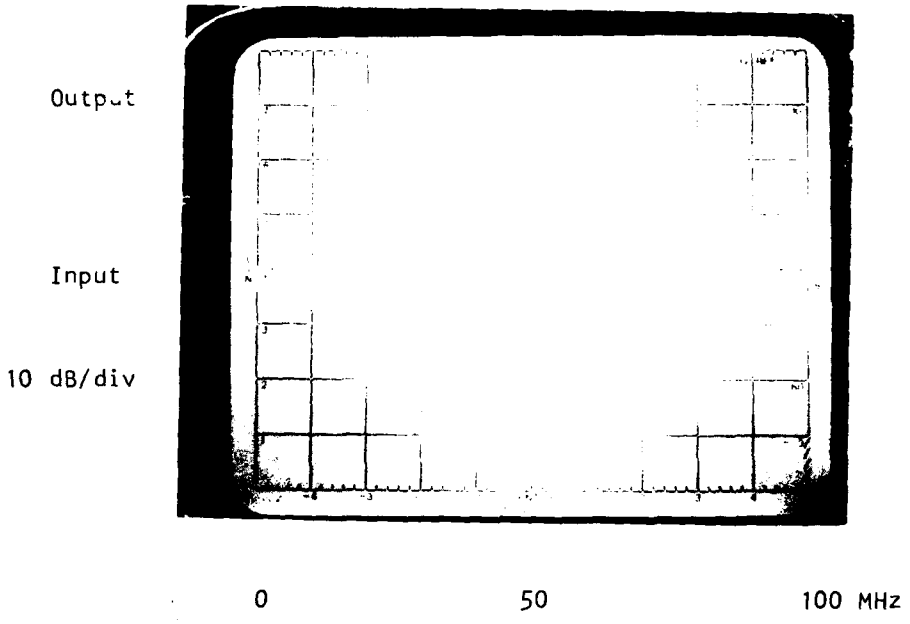


Figure 21 Frequency Response Characteristics of an SN7511 Video Amplifier Showing Output (Upper) and Input (Lower) Responses. (Scale factors: vertical, 10 dB/div; horizontal, 10 MHz/div.)

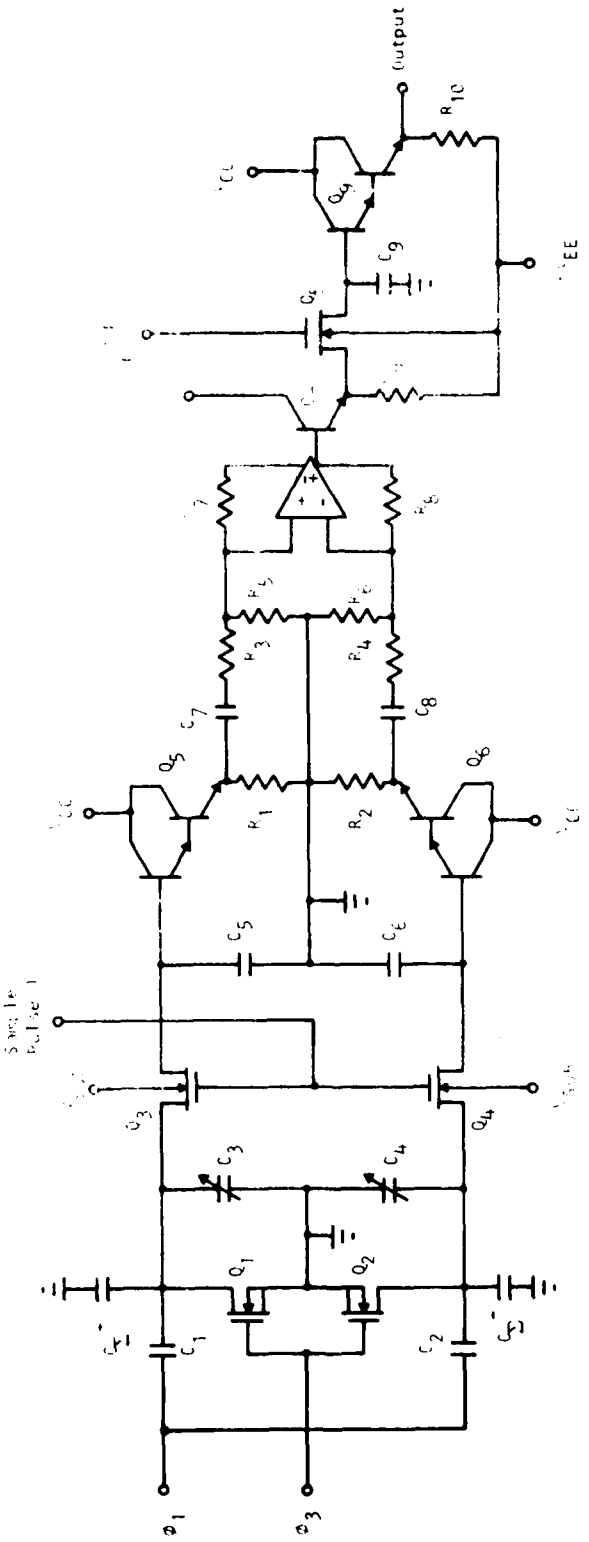
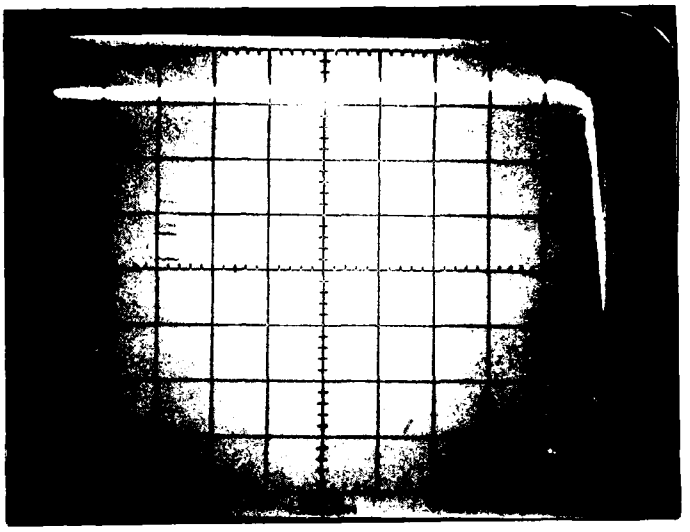


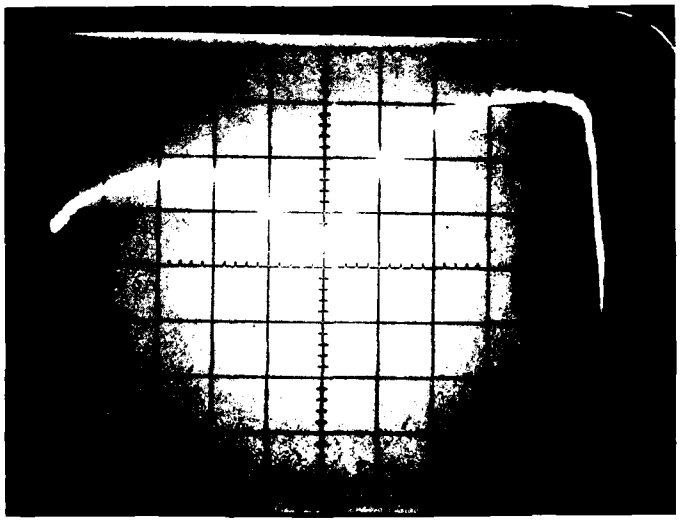
Figure 22 Differential Current Integrator and Sample-and-Hold Circuitry Utilized in Breadboard

C_1 and C_2, which integrate the transient clock currents. Variable capacitors C_3 and C_4 permit balancing of the stray capacitance to equalize the slight attenuation differences that may be experienced due to imbalances. During the off period of ϕ_1, transistors Q_1 and Q_2 provide a low impedance path to ground for the weighted clock lines to avoid any shift of dc level on the clock potential due to leakage from the sampling circuit. Transistors Q_3 and Q_4 and capacitors C_5 and C_6 form a pair of sample-and-hold circuits that are buffered by the Darlington emitter-followers composed of transistors Q_5 and Q_6. Symmetry is a very important consideration in this sample-and-hold circuitry to achieve good common mode rejection of the sampling pulse. Parasitic gate-to-source capacitance of transistors Q_3 and Q_4 in conjunction with C_5 and C_6 form capacitive voltage dividers for the sampling pulse. Differences in the capacitive sampling pulse feedthrough are treated as signal by the differential amplifier A_1 and emitter-follower Q_7 and R_9, which may result in a severely distorted waveform at the amplifier output. This distortion is further reduced by a second sample-and-hold function performed by transistor Q_8 and capacitor C_9 and buffered by the Darlington emitter-follower Q_9. The control pulse for this second sample-and-hold function also causes a similar parasitic feedthrough problem. The gain achieved in amplifier A_1 and the ability of this circuit to operate with a lower amplitude control pulse reduce the significance of the problem at this location.

The frequency response of much of the DCI was evaluated by injecting a swept signal at the base of Q_5 and observing the response in the succeeding stages. Figure 23 indicates the response of amplifier A_1 over the frequency range from 0 to 10 MHz. Figure 23(b) indicates the response of the circuit from the base of Q_5 to the emitter of Q_9 for the same input level as for the response in Figure 21(a). Approximately 2 dB loss is incurred at low frequencies in the sampling and buffering operations. The $(\sin \pi f/f_c)/(\pi f/f_c)$ sampling characteristic is readily apparent from Figure 23(b) where f_c = 5 MHz.



(a)



(b)

Figure 23 DCI Frequency Response (0 to 10 MHz). (a) Amplifier response; (b) amplifier and second sample-and-hold circuit. (Scale factors: vertical, 10 dB/div; horizontal, 1 MHz/div).

5. Clock Drivers

The total clock line capacitance for the four filters of Figure 10 is approximately 100 pF per phase. The CV^2f dissipation and waveform rise and fall times are important considerations for clock drivers capable of driving the CCD filters. The SN75361 MOS drivers are capable of operating at the desired frequency with the desired load capacitance, but they become quite warm, since they are incapable of large power dissipation due to packaging. To solve this problem, SN75361 chips were mounted in a dual in-line audio amplifier package that has heat-sink "wings" that safely dissipate the CV^2f power without excessive chip heating problems.

Figure 24 shows the clock waveforms generated within the breadboard. The upper trace is the 10 MHz master clock input, and the four lower traces are the 5 MHz output clock waveforms beginning with ϕ_1 and continuing through ϕ_4 at the bottom. These waveforms differ from the desired waveform slightly, in that the first half of the pulse suffers from a degraded amplitude. This degradation is due to capacitive coupling between clock drivers through the CCD clock electrode overlap capacitance.

6. Chirp Generation

Early in the program, the premultiply and postmultiply chirps were generated using a sweep generator. This proved to be unsatisfactory because of problems with synchronizing the sweep generator.

A satisfactory technique for chirp generation was supplied by NUC. R. W. Means, of NUC, constructed a chirp generator by coding each of the 32 required samples into 8 bits. An entire waveform could therefore be stored in a single 256-bit PROM. Harris 8256 256-bit PROMs were used in conjunction with Analog Devices 8-bit D/A converters. Two PROMs and two D/A converters were required for the generation of SIN and COS premultiply signals, and the system was duplicated for the postmultiply chirp.

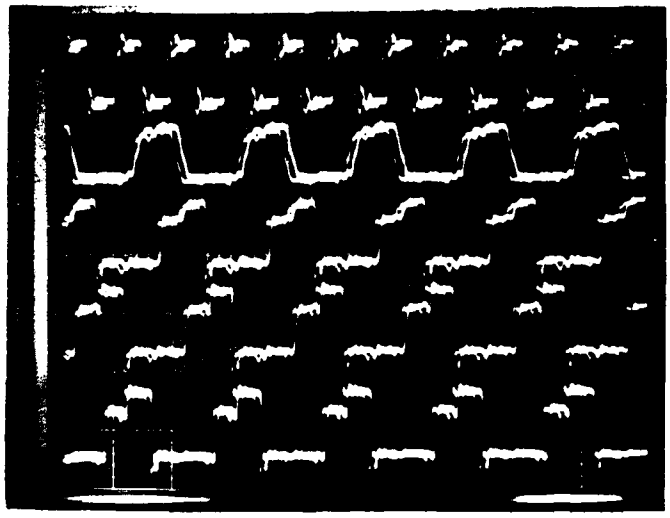


Figure 24 5 MHz Clock Waveforms Generated in Breadboard

The output from the postmultiply chirps is shown in Figure 16. The premultiply signals are identical except that the first sample in the COS waveform is $h_1 = 0.5$ instead of $h_1 = 1$.

C. Breadboard Results

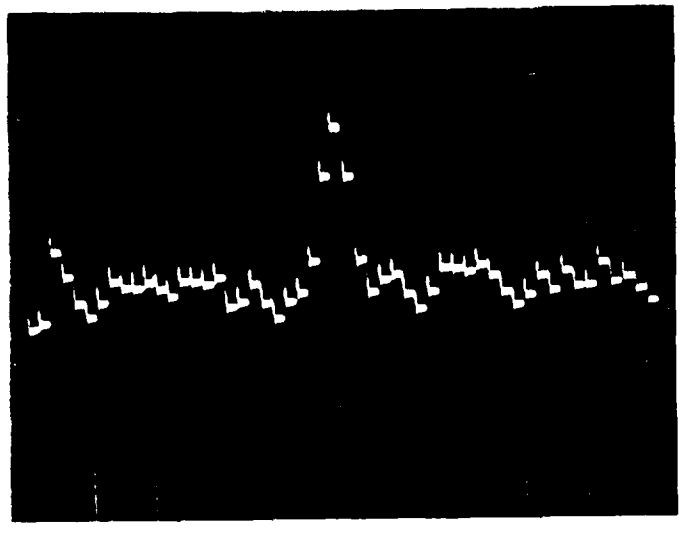
Figure 25 shows the output of the lower of the two DCIs shown in Figure 10. The clock rate is 1 MHz, and a dc level is applied to the input. The output shown is the correlation of the COS premultiply chirp with the COS filter response plus the correlation of the SIN premultiply chirp with the SIN filter response.

The breadboard output was evaluated by applying single frequency sinusoids to the inputs. For input signals of the form

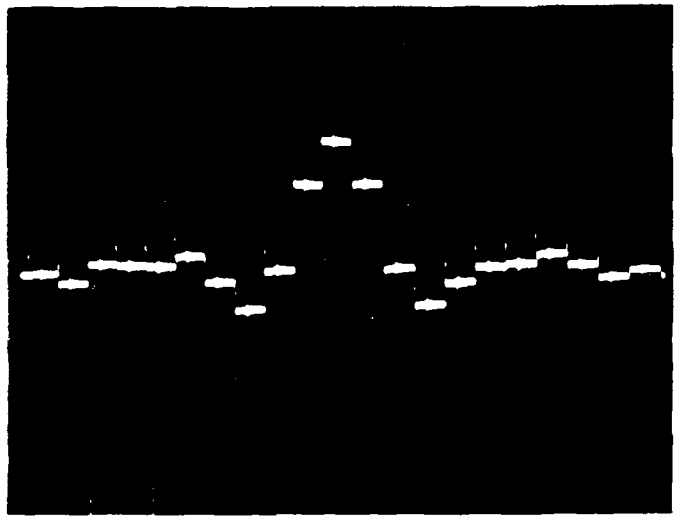
$$v_n = \cos\left(\frac{\pi Mn}{63}\right) \quad n = 1, 32, \tag{7}$$

the cosine transform is an impulse at $k = M$ for M integral. For $M = 0$, the impulse is 63 units high, whereas for $M \neq 0$, it is 31.5 units high. For M nonintegral, the cosine transform is complicated, and for any phase other than that of Equation (7) the simple impulse output disappears. Figure 26 shows the calculated cosine transform for a number of waveforms.

The result of inputting single frequency sinusoids is shown in Figure 27. The time scale in this series of photographs is adjusted so that the input chirp waveform occurs during the second through the fifth major time division. The input signal was gated to occur with coherent phase during this time period. The exact time of the end of the input waveform is unimportant, since the chirp waveform has 32 zero values after its 32 waveform values, and the multiplier output is zero during the chirp blanking period regardless of the input. Figures 27(a) through 27(f) show the breadboard output for inputs varying from dc to



(a)



(b)

Figure 25 Filter Correlation Characteristics at 1 MHz. Shown with (a) Compressed and (b) Expanded Time Scales

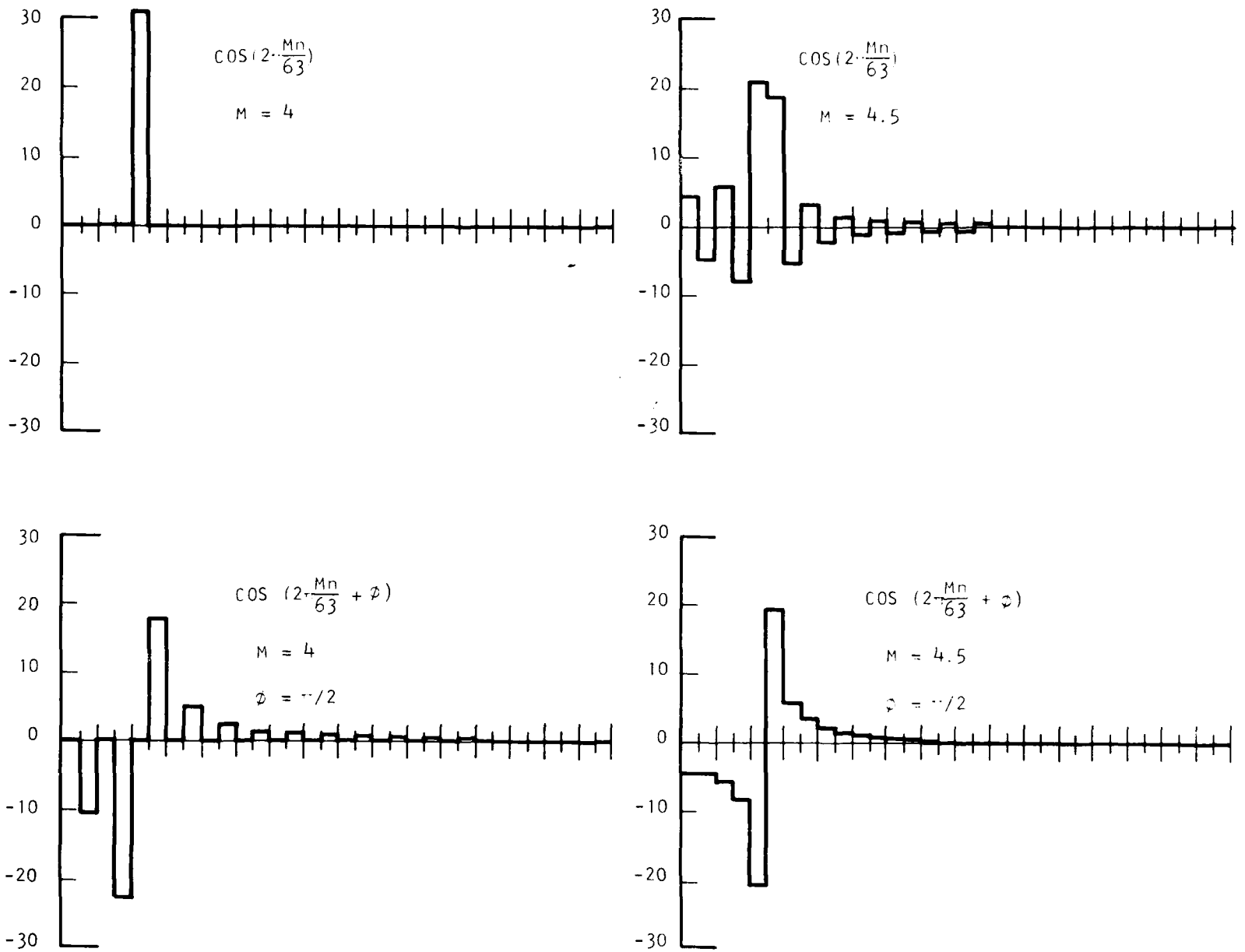


Figure 26 Calculated Cosine Transform of a Number of Sinusoidal Waveforms. When M is integral, and $\phi = 0$, the cosine transform is an impulse.

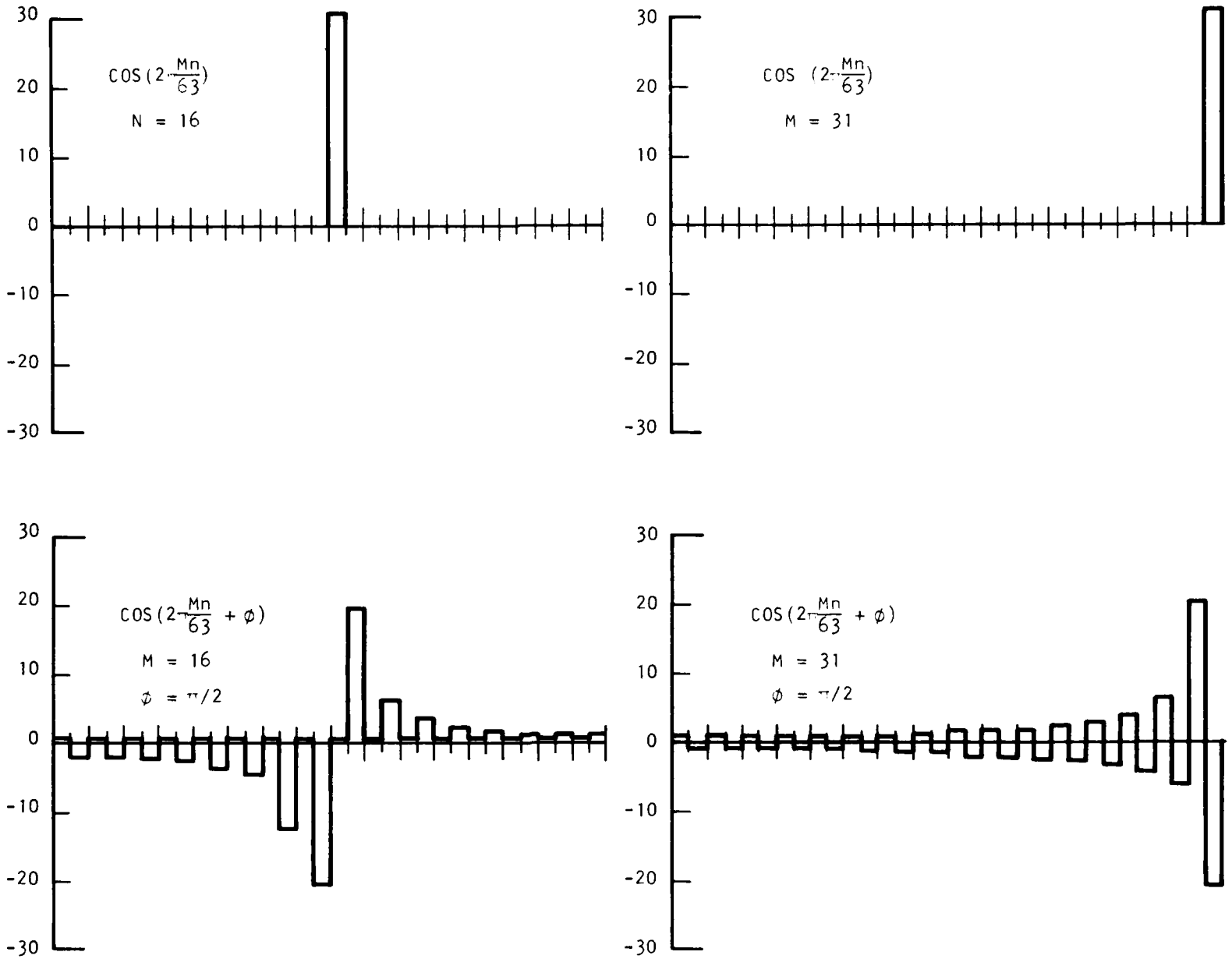


Figure 26 (continued) Calculated Cosine Transform of a Number of Sinusoidal Waveforms. When M is integral, and $\phi = 0$, the cosine transform is an impulse.

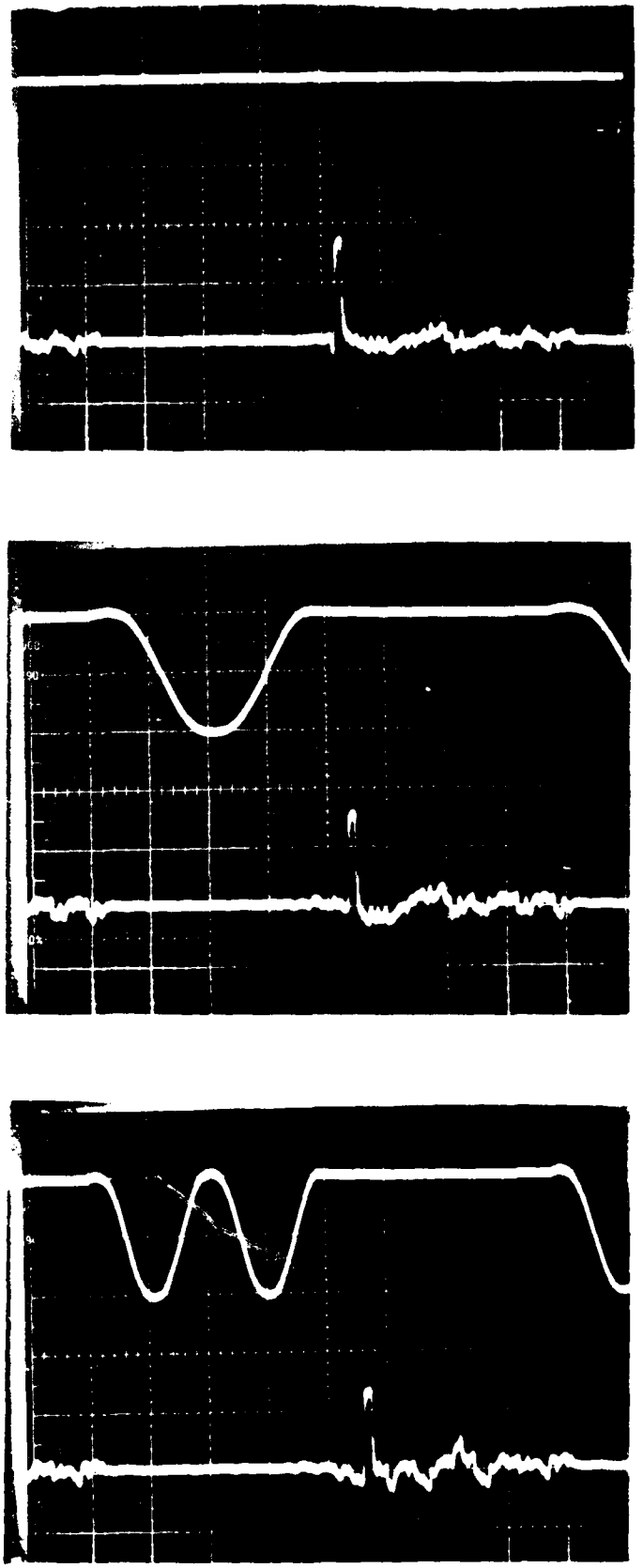
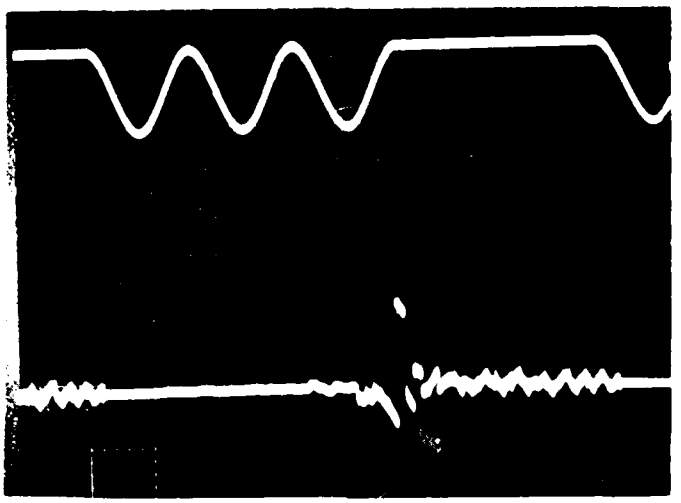
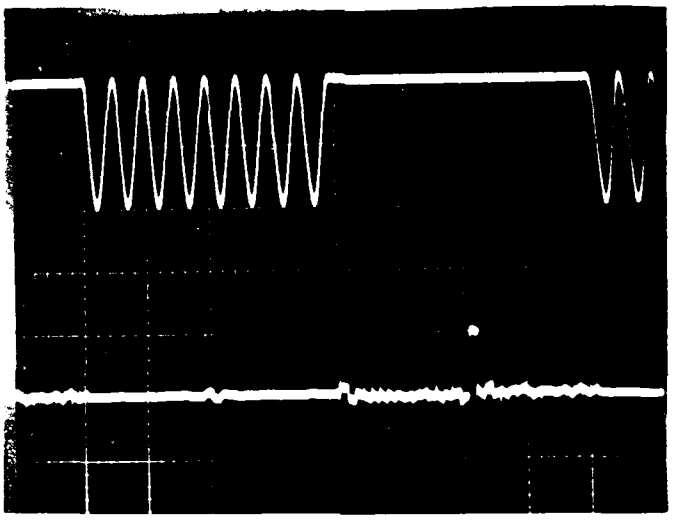
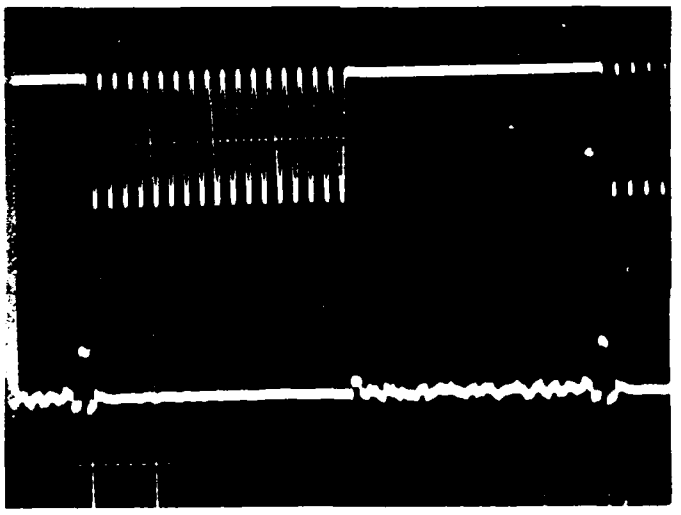


Figure 27 Cosine Transform Response at 1 MHz Clock Rate for (a) Dc and Gated Sinusoids at (b) 31.25 kHz and (c) 62.5 kHz





(e)



(f)

Figure 27 (cont'd) Cosine Transform Response at 1 MHz [illegible] Sinusoids at (d) 93.75 kHz, [illegible] and (f) 515.6 kHz

slightly above the Nyquist rate for a 1 MHz clock rate. For the cases shown, the output should be zero except for a single impulse. The non-zero elements in the outputs represent error in the system.

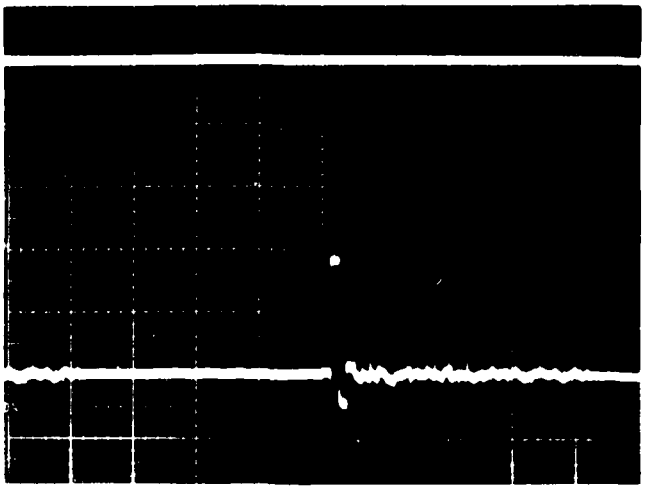
Figure 28 shows a similar set of results for 5 MHz operation. Charge transfer efficiency effects are more noticeable at 5 MHz, primarily through reduced correlation peak amplitudes.

The cosine transform cannot be interpreted in precisely the same way as the Fourier transform. However, there is a correspondence that is elucidated when a sinusoidal signal of arbitrary phase is applied to the input. The envelope that results from the superposition of many such outputs is shown in Figure 29(a) for the case M = 17 (f = 270 kHz, f_c = 1 MHz). Figure 29(b) shows a similar waveform for an amplitude-modulated signal. The carrier is 250 kHz and is almost 100% modulated by a 130 kHz sinusoid. In both cases, the photographs reflect the spectral content of the signals.

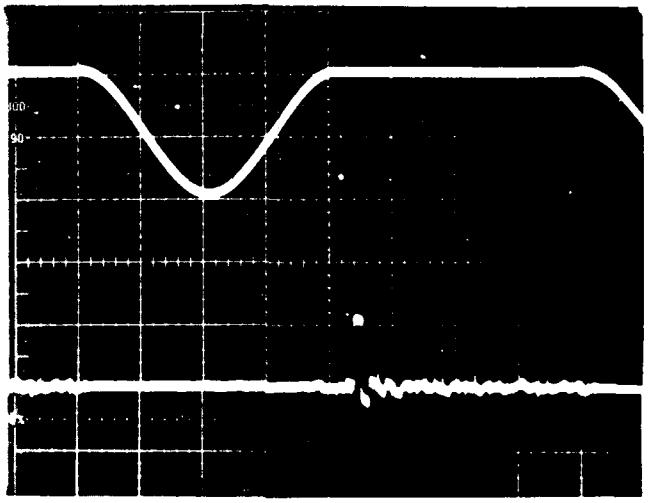
Figures 30 and 31 show the breadboard response to square waves and to a triangular wave. In Figure 30(a), the dc (M = 0), fundamental (M = 5), first harmonic (M = 10), second harmonic (M = 15), and third harmonic (M = 20) are visible. In Figure 30(b) only the dc (M = 0) and odd harmonics (M = 5, M = 15) are present. For the triangular wave of Figure 31, the fundamental corresponds to M = 6.

The breadboard has also been evaluated by looking at its impulse response. The cosine transform of an impulse located in the Nth time slot (N = 0, 31) is a cosine having frequency N/63. If the input waveform is

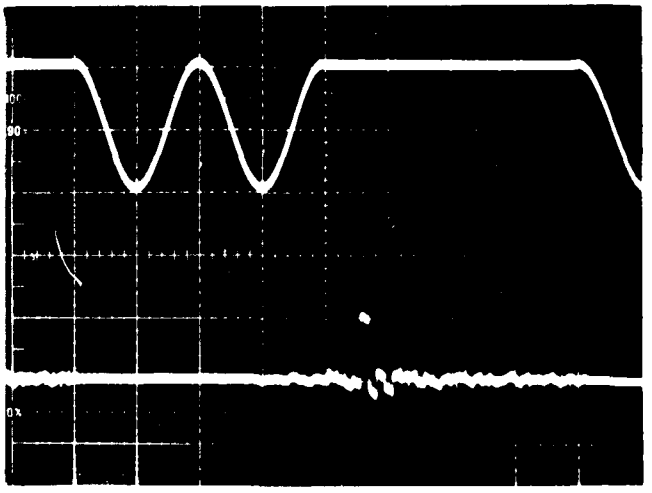
$$v_n = \begin{cases} 1 & n = N \\ 0 & n \neq N \end{cases}, \qquad (8)$$



(a)

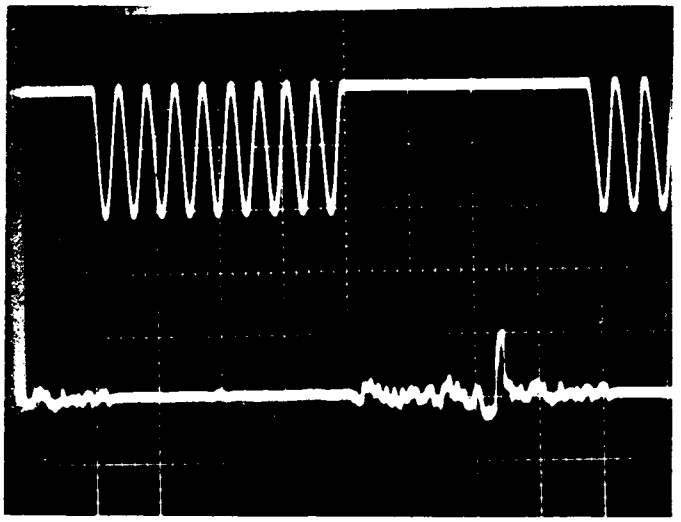


(b)

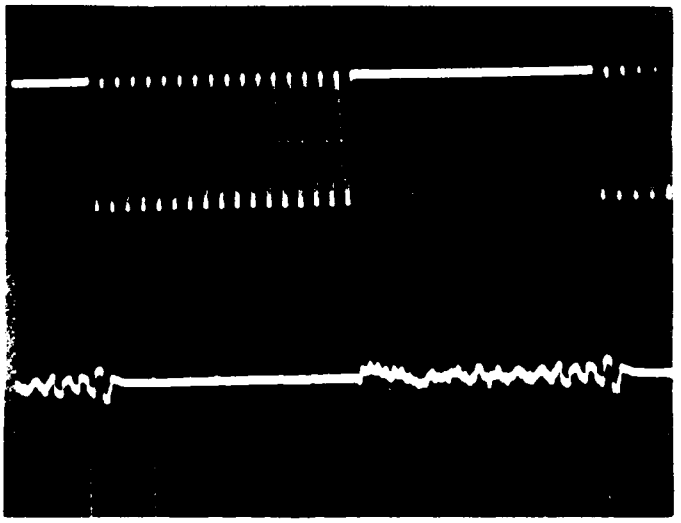


(c)

Figure 28 Cosine Transform Response at 5 MHz Clock Rate for (a) dc and Gated Sinusoids at (b) 156.25 kHz and (c) 312.5 kHz

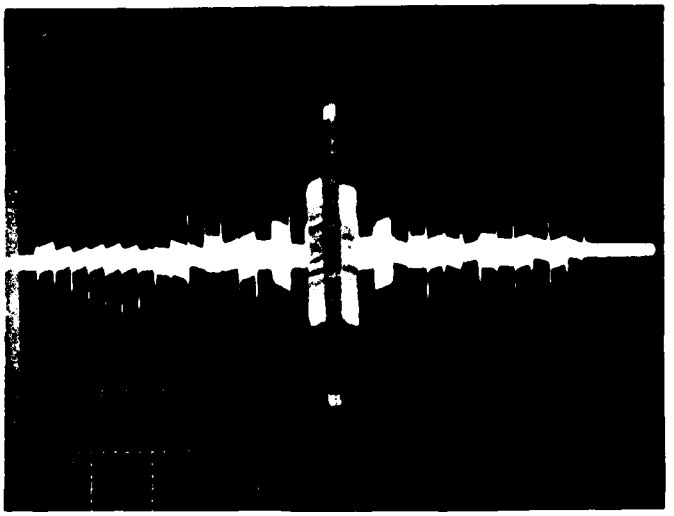


(d)

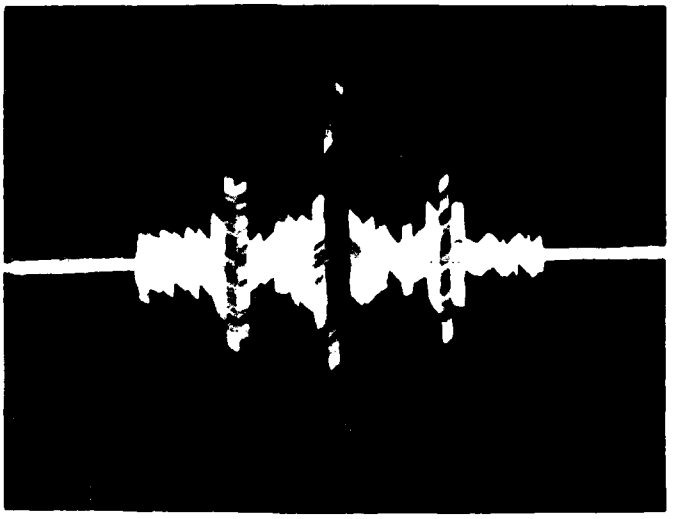


(e)

Figure 28 (cont'd) Cosine Transform Response at 5 MHz Clock Rate for Gated Sinusoids at (d) 1.406 MHz and (e) 2.578 MHz

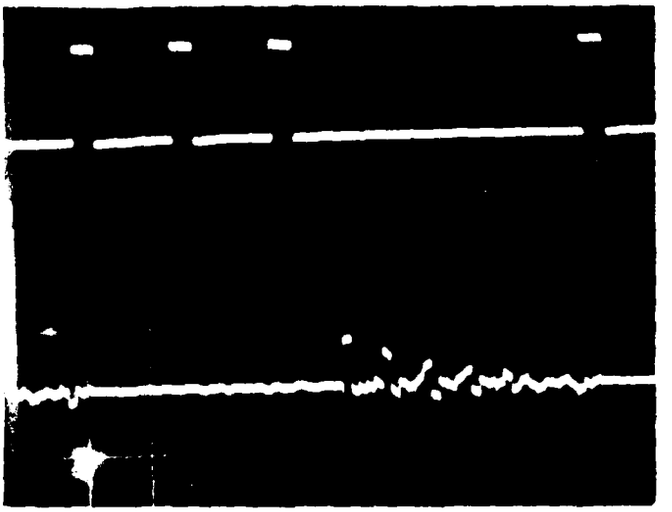


(a)

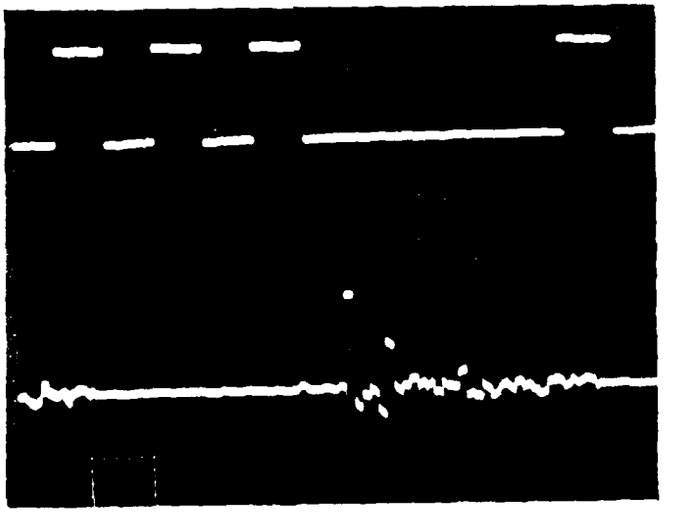


(b)

Figure 29 (a) Cosine Transform of a 270 kHz Sinusoid of Arbitrary Phase.
(b) Cosine Transform of an AM Signal of Arbitrary Phase.



(a)



(b)

Figure 30 Breadboard Response to (a) Rectangular and (b) Square Wave Pulse Trains

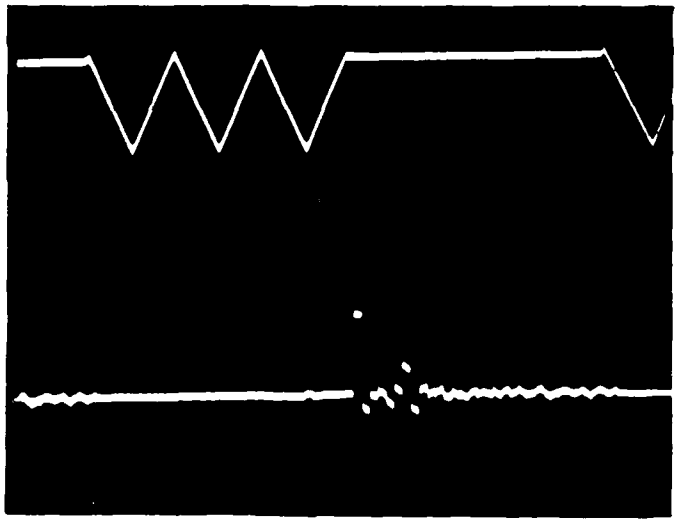
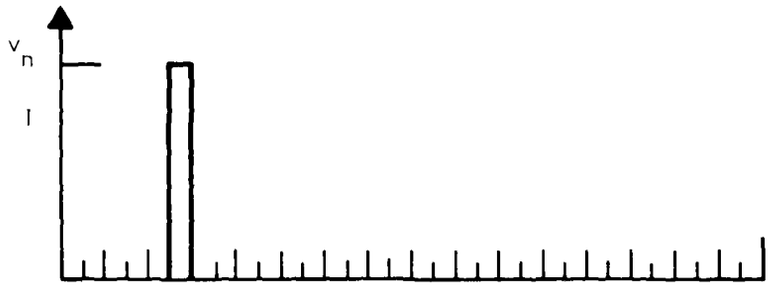


Figure 31 Breadboard Response to a 93.75 kHz Triangular Wave Train

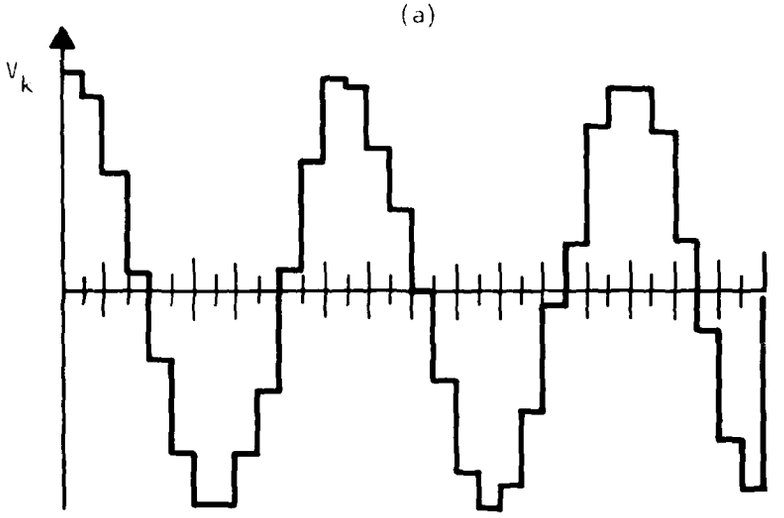
then the cosine transform is

$$V_k = \cos 2\pi \frac{Mk}{63} . \tag{9}$$

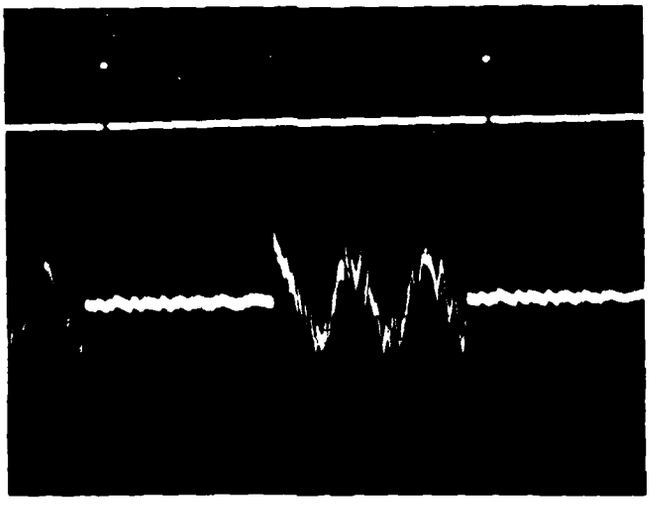
Figure 32 shows the calculated and observed cosine transform of an impulse at N = 5.



(a)



(b)



(c)

Figure 32 (a) Impulse at N = 5; (b) Calculated Cosine Transform of (a); (c) Observed Cosine Transform of an Impulse at N = 5.

SECTION IV

CONCLUSIONS

The bucket brigade device (BBD) has been successfully incorporated by Robert W. Means of NUC into a breadboard bandwidth reduction system for a 100 x 100 imager. The video information is processed at 5 frames per second, which corresponds to a 50 kHz clock rate in the BBDs. The BBD breadboard has been very effective in demonstrating the bandwidth compression concept; however, the BBDs are not capable of operating at the 5 MHz that is required for the ultimate application of these devices.

The CCD breadboard was undertaken with two goals in mind: (1) operation at 5 MHz, and (2) integration of multipliers and DCI. These goals were not achieved simultaneously. Operation at 5 MHz required discrete bipolar multipliers and a discrete DCI.

In the process of breadboarding the DCI, a new design was used, and computer simulation indicates that an integrated version of this DCI will operate well at 5 MHz. For the analog multipliers, however, a new approach must be found. Several new approaches have been proposed, but none has yet been demonstrated to work at 5 MHz.

By far the most difficult part of the contract effort was making the breadboard operate at 5 MHz. At 1 MHz, waveforms throughout the system are clean, and adjustments are noncritical that become much more critical at 5 MHz.

At present, the 5 MHz multiplier appears to be the major problem to be solved. Several approaches are being explored, the most promising of which is a D/A multiplier that multiplies an analog signal by a digital signal to produce an analog output. The importance of this component was pointed out by Harper Whitehouse, and preliminary design and simulation are encouraging.

It is our strong recommendation that the continuous chirp z-transform[8] be explored for the bandwidth reduction application. This transform has the advantage of extreme simplicity of implementation: (1) for an N-point transform the CCD filters need have only N stages; (2) the filters operate with 100% duty cycle so that only one CZT is required instead of two; (3) the premultiply and postmultiply chirp waveforms are identical; and (4) the system is less sensitive to charge transfer loss.

In summary, the results of Contract No. N00123-74-C-1366 were mixed. The BBDs work very well, and the CCD breadboard works well at low frequency. However, the high frequency operation of the CCD breadboard presented more problems than were anticipated at the beginning of the program. The integrated multipliers and DCI failed to operate at 5 MHz, and discrete implementations of these functions were used to achieve 5 MHz operation. However, a great deal was learned under the contract that will enable us to design 5 MHz components into future CZT systems.

REFERENCES

1. H. J. Whitehouse, J. M. Speiser and R. W. Means, "High Speed Serial Access Linear Transform Implementations," presented at the All Applications Digital Computer Symposium, Orlando, Florida, 23-25 January 1973. NUC TN 1026.

2. R. W. Means, D. D. Buss, and H. J. Whitehouse, "Real Time Discrete Fourier Transforms Using Charge Transfer Devices," Proc. CCD Applications Conference, San Diego, pp. 127-139, September 1973.

3. R. W. Means, H. J. Whitehouse, and J. M. Speiser, "Television Encoding Using a Hybrid Discrete Cosine Transform and a Differential Pulse Code Modulator in Real Time,"

4. Technical Report RADC-TR-73-259, June 1973, "Investigation of Semiconductor Charge Devices Part II: Breadboard Fabrication and Testing" by D. D. Buss and W. H. Bailey.

5. D. D. Buss, D. R. Collins, W. H. Bailey, and C. R. Reeves, "Transversal Filtering Using Charge Transfer Devices," IEEE J. Solid-State Circuits SC-8, 138 (1973).

6. F. Bonzanigo, "A Note on Discrete Hilbert Transform," IEEE Trans. Audio and Electroacoustics AU-20, 99 (March 1972).

7. B. Gilbert, "A Precision Four-Quadrant Multiplier with Subnanosecond Response," IEEE J. Solid-State Circuits SC-8, 365 (1968).

8. R. W. Brodersen, H. S. Fu, R. C. Frye, and D. D. Buss, "A 500-Point Fourier Transform Using Charge-Coupled Devices," 1975 IEEE ISSCC Digest of Technical Papers, to be published.

MINI-RPV ENCODER/DECODER
FINAL TECHNICAL REPORT

G. Graham Murray
Data/Ware Development Inc.

DATA/WARE DEVELOPMENT INC.
11585 SORRENTO VALLEY ROAD
SUITE 108
SAN DIEGO, CA 92121

(714) 453-7660

T-75-766

COMPUTER SYSTEMS, APPLICATIONS, IMPLEMENTATION

July 22, 1975

MINI-RPV ENCODER/DECODER

FINAL TECHNICAL REPORT

Contract #N66001-75-C-0218

Prepared for
Naval Undersea Center
Code 602
San Diego, California

CONTENTS

FIGURES

CONTENTS - Continued

FIGURES

TABLES

MINI-RPV ENCODER/DECODER DETAILED LOGIC DESIGN

1. Introduction

For the mini-RPV application under consideration, digitized and compressed video from a TV camera will be encoded to permit reliable operation over a noisy communications channel. The encoded output is processed through a spread spread video modem and transmitter. At the receiving site, the modem output is routed to a Maximum-Likelihood Decoder, after which the received data enters the TV display system. The encoder/decoder employs Reed-Muller codes and is able to adapt to different compression ratios in the TV system. In every case the encoder outputs a bit stream at 1600 KHz. This data is passed to the modem as 4-bit characters at 400 KHz.

The encoder controls the generation of code words in the modem which consist of signed "base vectors" identified as A, B, C, ..., H. The chip patterns for each base vector are supplied by the modem. Therefore the encoder need furnish only 4-bit characters, each of which is interpreted as a sign and a base vector identification, i.e. as ±A, ±B, ---, ±H. The bit stream entering the encoder from the TV system is organized into 8-bit characters. For each such character, the encoder generates a "compound" vector which consists of a series of signed base vectors. See Table 1-1.

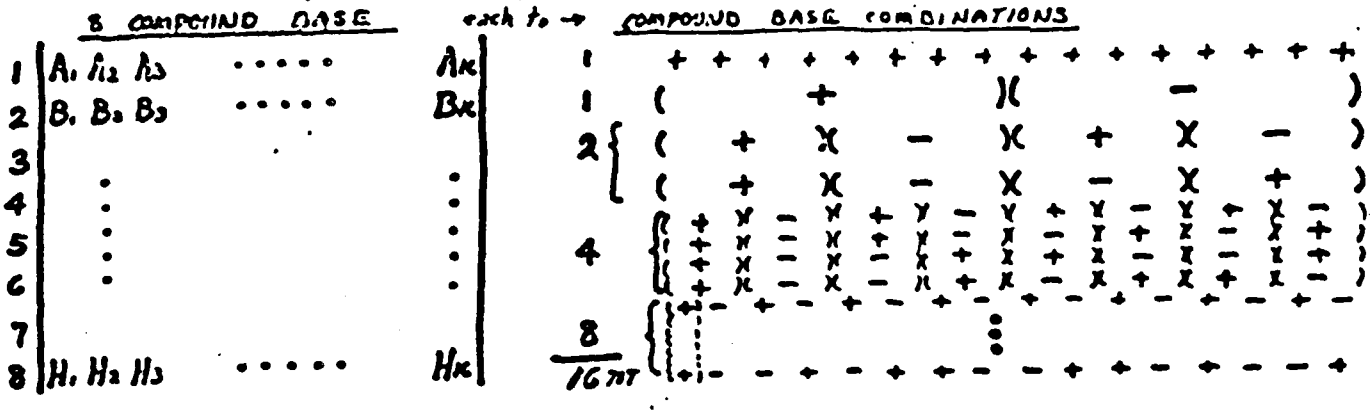
To permit different amounts of data compression, there are four Formats. Table 1-1 shows the first three, corresponding to input data rate of 200, 400, and 800 kbps. There is also available a fourth Format, which is uncoded at 1.6 Mbps. Regardless of the input data rate, the output data rate of the encoder is 1.6 Mbps (4-bit characters at 400 KHz). Figure 1-1 shows the encoder's relationship to the TV imagery system and to the modem. The serial bit stream from the TV system is clocked in by the encoder, with the convention that on the rising edge of

Table 1-1 Code Formats

Code Format I

200K video data = 25K words/sec × 8 bit words

25K words/sec. × 32 chip base vector × 16 base vectors/word = 12.8 M chips/sec.

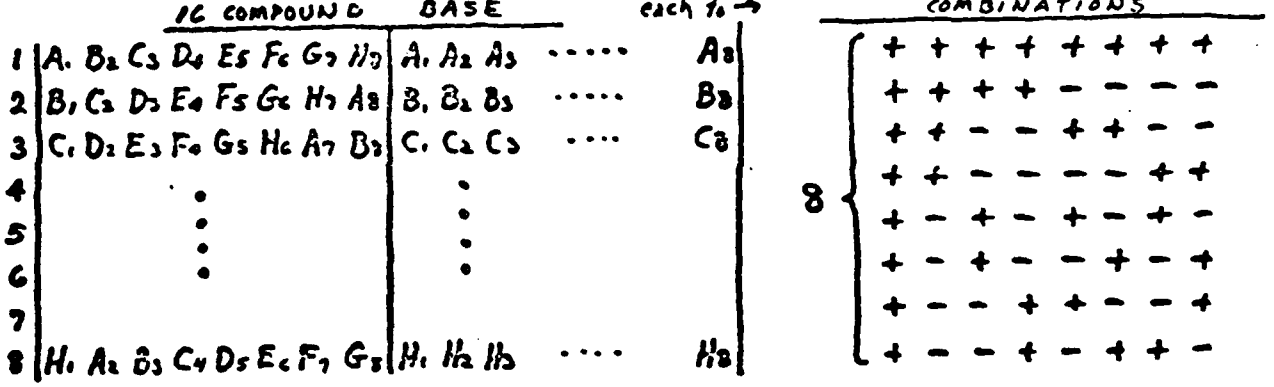


8 compound base vectors × 16 combinations each × 2 bipolar = 256 states required

Code Format II

400K video data = 50K words/sec. × 8 bit words

50K words/sec. × 32 chip base vector × 8 base vectors/word = 12.8 M chips/sec.

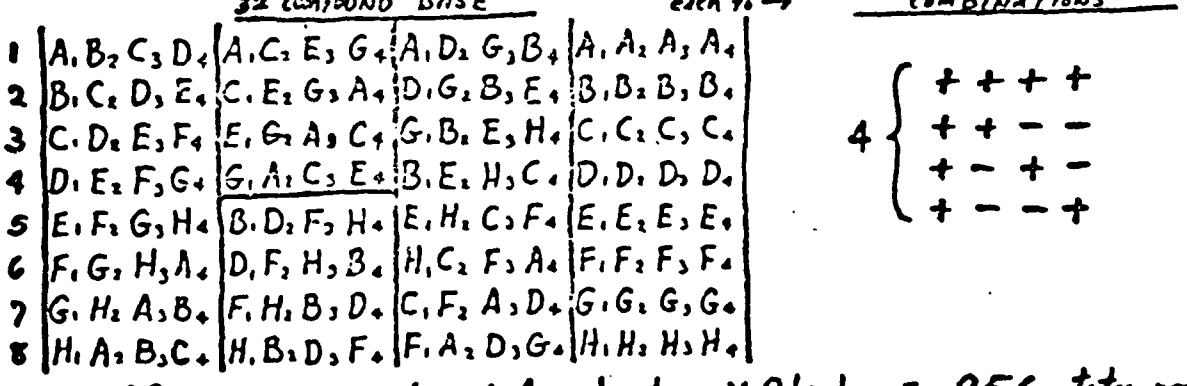


16 compound base vectors × 8 combinations each × 2 bipolar = 256 states required

Code Format III

800K video data = 100K words/sec. × 8 bits/word

100K words/sec. × 32 chip base vectors × 4 base vectors/word = 12.8 M chips/sec.



32 compound base vectors × 4 combinations × 2 bipolar = 256 states required

the clock the TV system issues the next bit and on the falling edge the data is strobed into the encoder.

The modem provides the encoder with two control and four timing signals:

x, y: Coded to indicate the Format (I, II, III or IV)
The code is 00, 01, 10, 11 respectively

Master Clock: 12.8 MHz square wave.
Word Clock: 25, 50, 100, or 200 KHz square wave.
Sampling Clock: 400 KHz square wave.
Bit Clock: 200, 400, 800 or 1600 KHz square wave.

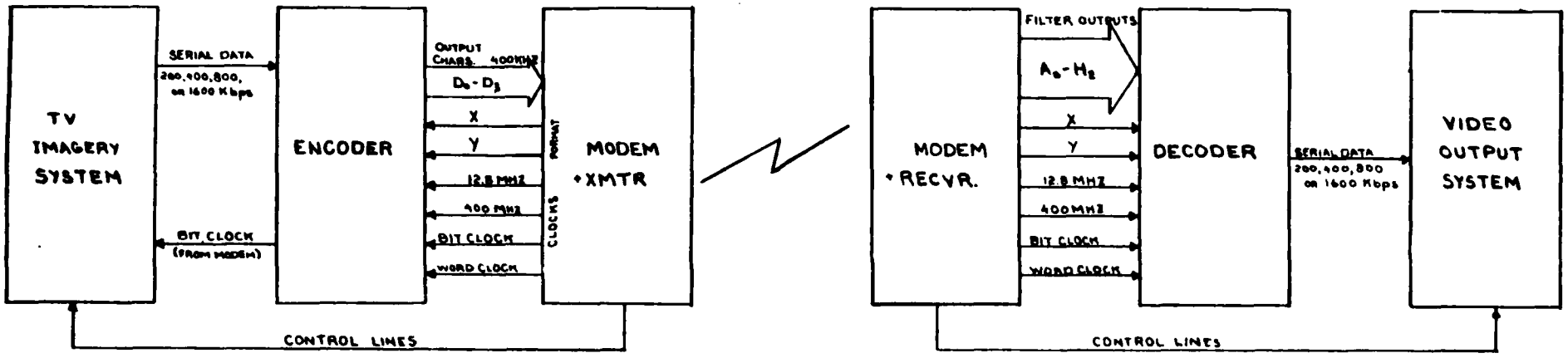
The output of the encoder to the modem consists of four data lines each transmitting a bit of information. Three of the bits indicate a "base vector", A thru H, together with the fourth bit indicating the base vector's sign. The trailing edge of the 400 KHz clock is used at the modem to sample the encoder output, identified as bits D_0 to D_3.

The encoder blocks the incoming data into 8-bit characters by means of the Word Clock generated by the modem. Then, depending upon the format, the data will be encoded to the appropiate code outputted to the modem in 4-bit bytes a Word Clock latter.

At the receiving site the decoder processes the modem output and provides data to the video display system. Whereas the encoder passes 400 KHz 4-bit characters to the modem, at the receiving end the modem delivers 8 3-bit characters to the decoder. The reason is that the modem output is expressed in terms of the "base vectors", A thru H. The modem does not make a decision as to which of the 8 received base vectors was exciting its corresponding filter the most, but instead expresses the amount of excitation as a 3-bit binary number and transmits all 8 numbers to the decoder. During the decoding process, the decoder

will determine the "most likely" code that excited the modem's filters corresponding to all possible 8-bit input characters. In the first three formats the decoder has 256 possible combinations of 8 bit characters to consider in determining the most likely one. In Format IV there is no coding involved, and the decoder simply determines the largest absolute value of the 8 modem outputs. The maximum likelihood 8-bit character selected from the correlation process will be outputted to the video terminals at a rate consistent with the particular format (200 KHz (bits per second) for Format I, 400 KHz for Format II, 800 KHz for Format III, and 1600 KHz for Format IV.

From the modem the 8 3-bit words are clocked on the rising edge of the word clock into the decoder, all in parallel at a 400 KHz rate. The output of the decoder to the video system consists of a serial stream of bits which comprise the decoded video information. The decoder outputs data after a delay of three word clocks, valid on the falling edge of the bit clock, least significant bit first. As with the encoder, the clock and control signals are generated by the modem.



TV SYSTEM

FIGURE 1-1

2. Encoder Theory

2.1 General Description

The encoder accepts 8-bit words, serially on a single line, from the video system. It encodes the information and retransmits it, 4 bits at a time on 4 parallel lines, to the modem.

The encoder operates in one of four different formats, I, II, III, and IV. The input data rate to the encoder varies with the format, but the output data rate is always the same.

In Formats I, II, and III, the input data rate is lower than the output data rate, and the encoder adds redundancy to the information, transmitting more bits than it receives. The information is "spread" in time and among the bits, so that if some bits are lost after leaving the encoder, the information may still be retrieved in the decoder.

In Format IV the input and output data rates are equal, and there is no redundancy in the output information.

2.2 Interface Description

Figure 2-1 is an interface diagram of the encoder, and Figure 2-2 shows the timing for the four different formats.

The Format signals, X and Y, select the format in which the encoder operates, according to the table in Figure 2-1. The Word Clock, Data Bit Clock, and Input Data rates are all adjusted by the external system, not by the encoder, to conform to the table in Figure 2-1.

The Data Bit Clock is used by the encoder to sample the Input Data.

The Input Data signal contains the serial input data; the bits of each 8-bit word are called X0 (the first bit of each word to be received) through X7 (the last bit). The data changes at the

rise of the Data Bit Clock and for a while thereafter. It is stable and is sampled by the encoder at the fall of the Data Bit Clock. Bit X0 is present at the fall of the Data Bit Clock next following the rise of the Word Clock.

The Word Clock is used by the encoder to determine the grouping of the Input Data into 8-bit words, and also defines the time slots for the Output Data, as described below.

The 400 KHz Clock is used by the encoder as its internal clock, and defines the time when output data may be sampled by the external system, as described below.

The 12.8 MHz Clock is brought to the encoder and terminated there (as are the other three clocks), but is not functionally used by the encoder.

The Output Data signals, D0 through D3, are the encoder outputs. They change at the rise of the 400 KHz Clock and for a while thereafter; they are stable and may be sampled by the external system at the fall of the 400 KHz Clock. The Output Data signals for time slot 00 (T00), as described below, are present at the fall of the 400 KHz Clock next following the rise of the Word Clock.

2.2.1 Timing

For each 8-bit input data word X0-X7, a corresponding series of 4-bit outputs is delivered in time slots (of the 400 KHz Clock) starting with 00 and ending with 15, 07, 03, or 01 (all base 10), depending on the format, as shown in Figure 2-2.

Regardless of format, the encoder always introduces a one-word delay between the input and output data; that is, when Word n is coming into the encoder, Word n-1 is being transmitted (Figure 2-2).

In any of the preceding or following descriptions of timing, references to signals pertain to the signals as seen at the encoder terminals (the circuit board edge connector).

2.3 Transfer Functions

The encoder transfer function is different for each of the four formats, but the possible configurations of the Output Data bits D0-D3 are always defined as follows (See Figure 2-3):

D0 displays the sign, a logical "0" corresponding to a "+" (plus) and a logical "1" corresponding to a "-" (minus).

D1-D3 display one of the eight vectors A, B, C, D, E, F, G, H, according to the table in Figure 2-3.

Figures 2-4 through 2-7 define outputs D0-D3 as a function of inputs X0-X7, for Formats I through IV, respectively.

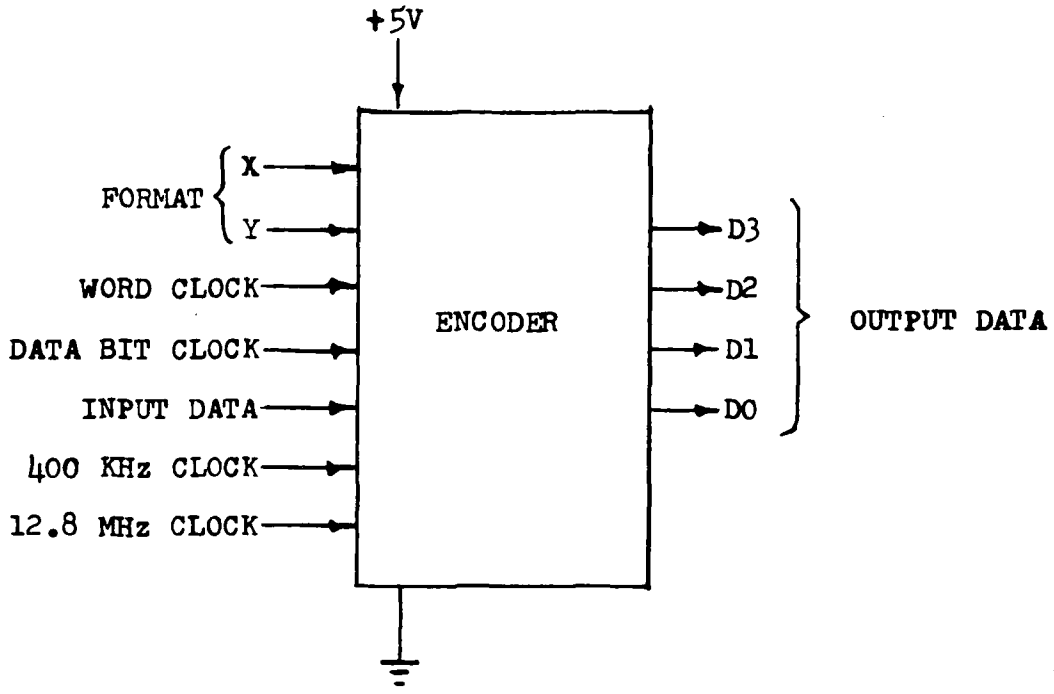
The number of output time slots (of the 400 KHz Clock) corresponding to each 8-bit input word is 16, 8, 4, or for Formats I, II, III, or IV, respectively.

In Formats I, II, and III, output D0 is the result of an Exclusive-OR operation between input bit X0 and a function dependent on the other input bits which define the sign; in other words, when X0 is "1", output D0 is inverted from its configuration when X0 is "0".

In Format IV, outputs D0-D3 are simply X0 through X7 broken into two 4-bit groups, X0-X3 being transmitted first and X4-X7 being transmitted last.

Figure 2-8 is an example of the encoder operation for Format II, Formats I and III are similar.

Figure 2-9 is an example of operation for Format IV.



X	Y	FORMAT	DATA BIT CLOCK KHz	WORD CLOCK KHz
0	0	I	200	25
0	1	II	400	50
1	0	III	800	100
1	1	IV	1600	200

Notes: All clocks are synchronous, all rising at the rise of the word clock.

All clocks are square waves (50% duty cycle)

FIG. 2-1 - Encoder Interface Diagram

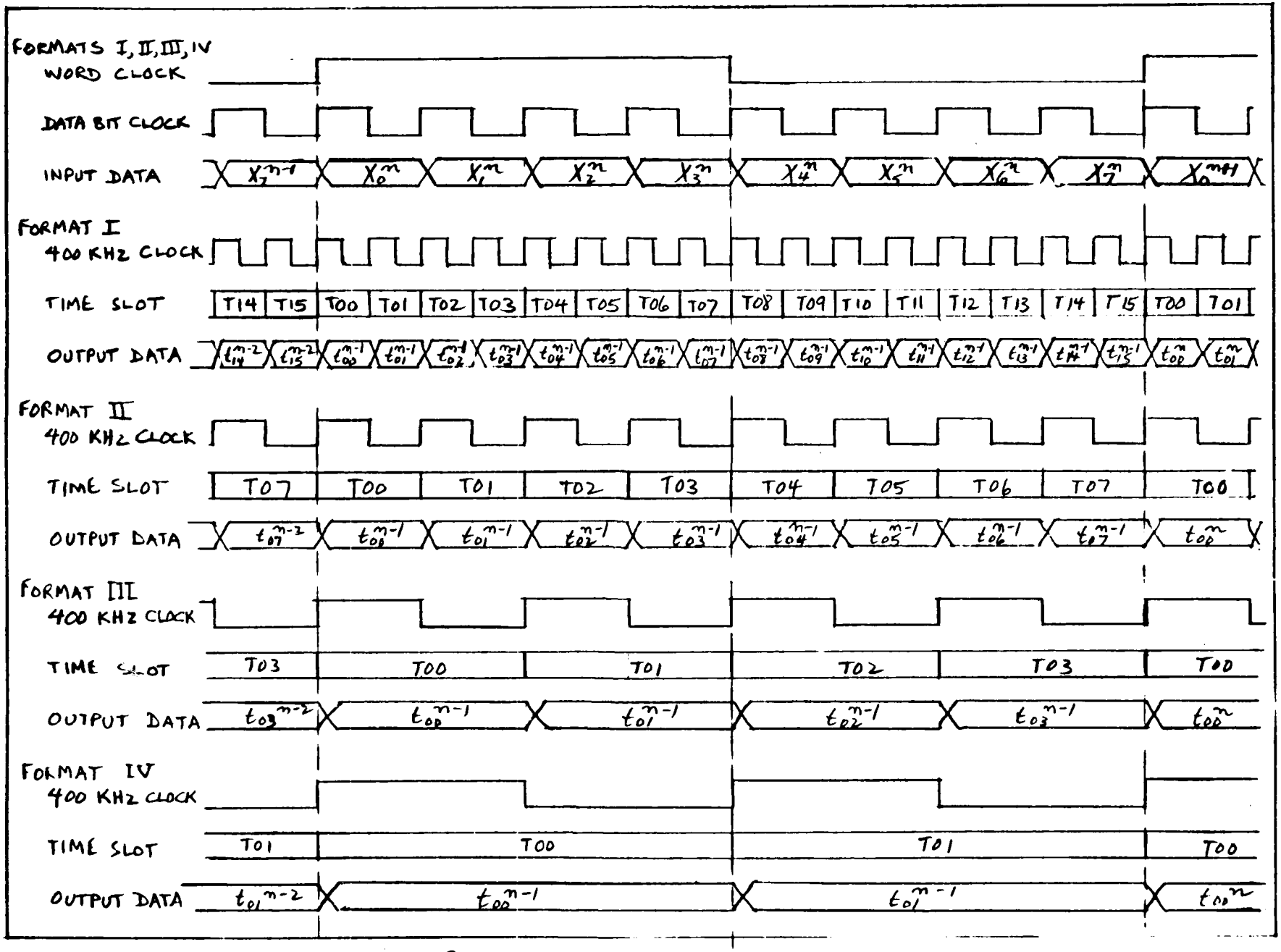


FIG. 2-2 - ENCODER TIMING

D3	D2	D1	Vector	D0	Sign
0	0	0	A	0	+ (plus)
0	0	1	B	1	- (minus)
0	1	0	C		
0	1	1	D		
1	0	0	E		
1	0	1	F		
1	1	0	G		
1	1	1	H		

FIG. 2-3 - Output Data Configurations

					OUTPUT TIME SLOT														
					0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
					0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5
X0	X6	X2	X1	X7	SIGN DO															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
0	0	0	1	0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
0	0	0	1	1	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0
0	0	1	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
0	0	1	0	1	0	1	0	1	1	0	1	0	0	1	0	1	1	0	1	0
0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
0	0	1	1	1	0	1	1	0	1	0	0	1	0	1	1	0	1	0	0	1
0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
0	1	0	0	1	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
0	1	0	1	0	0	0	1	1	0	0	1	1	1	1	0	0	1	1	0	0
0	1	0	1	1	0	0	1	1	1	1	0	0	1	1	0	0	0	0	1	1
0	1	1	0	0	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0
0	1	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0	0	1	0	1
0	1	1	1	0	0	1	1	0	0	1	1	0	1	0	0	1	1	0	0	1
0	1	1	1	1	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
1	0	0	1	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
1	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
1	0	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
1	0	1	0	1	1	0	1	0	0	1	0	1	1	0	1	0	0	1	0	1
1	0	1	1	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
1	0	1	1	1	1	0	0	1	0	1	1	0	1	0	0	1	0	1	1	0
1	1	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1	1
1	1	0	1	0	1	1	0	0	1	1	0	0	0	0	1	1	0	0	1	1
1	1	0	1	1	1	1	0	0	0	0	1	1	0	0	1	1	1	1	0	0
1	1	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1
1	1	1	0	1	1	0	1	0	0	1	0	1	0	1	0	1	1	0	1	0
1	1	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0	0	1	1	0
1	1	1	1	1	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

X5	X4	X3	VECTOR D1-D3 (See Fig. 3)
0	0	0	A A A A A A A A A A A A A A A A
0	0	1	B B B B B B B B B B B B B B B B
0	1	0	C C C C C C C C C C C C C C C C
0	1	1	D D D D D D D D D D D D D D D D
1	0	0	E E E E E E E E E E E E E E E E
1	0	1	F F F F F F F F F F F F F F F F
1	1	0	G G G G G G G G G G G G G G G G
1	1	1	H H H H H H H H H H H H H H H H

FIG. 2-4 - Format I Transfer Function

X0	X2	X1	X7	OUTPUT TIME SLOT 0	1	2	3	4	5	6	7	SIGN	D0
0	0	0	0	0	0	0	0	0	0	0	0		
0	0	0	1	0	0	0	0	1	1	1	1		
0	0	1	0	0	0	1	1	0	0	1	1		
0	0	1	1	0	0	1	1	1	1	0	0		
0	1	0	0	0	1	0	1	0	1	0	1		
0	1	0	1	0	1	0	1	1	0	1	0		
0	1	1	0	0	1	1	0	0	1	1	0		
0	1	1	1	0	1	1	0	1	0	0	1		
1	0	0	0	1	1	1	1	1	1	1	1		
1	0	0	1	1	1	1	1	0	0	0	0		
1	0	1	0	1	1	0	0	1	1	0	0		
1	0	1	1	1	1	0	0	0	0	1	1		
1	1	0	0	1	0	1	0	1	0	1	0		
1	1	0	1	1	0	1	0	0	1	0	1		
1	1	1	0	1	0	0	1	1	0	0	1		
1	1	1	1	1	0	0	1	0	1	1	0		

X6	X5	X4	X3	VECTOR D1-D3 (See Fig. 3)							
0	0	0	0	A	A	A	A	A	A	A	A
0	0	0	1	A	B	C	D	E	F	G	H
0	0	1	0	B	B	B	B	B	B	B	B
0	0	1	1	B	C	D	E	F	G	H	A
0	1	0	0	C	C	C	C	C	C	C	C
0	1	0	1	C	D	E	F	G	H	A	B
0	1	1	0	D	D	D	D	D	D	D	D
0	1	1	1	D	E	F	G	H	A	B	C
1	0	0	0	E	E	E	E	E	E	E	E
1	0	0	1	E	F	G	H	A	B	C	D
1	0	1	0	F	F	F	F	F	F	F	F
1	0	1	1	F	G	H	A	B	C	D	E
1	1	0	0	G	G	G	G	G	G	G	G
1	1	0	1	G	H	A	B	C	D	E	F
1	1	1	0	H	H	H	H	H	H	H	H
1	1	1	1	H	A	B	C	D	E	F	G

FIG. 2-5 - Format II Transfer Function

			OUTPUT TIME SLOT	SIGN DO
			0 0 0 0	
			0 1 2 3	
X0	X7	X6		
0	0	0		0 0 0 0
0	0	1		0 0 1 1
0	1	0		0 1 0 1
0	1	1		0 1 1 0
1	0	0		1 1 1 1
1	0	1		1 1 0 0
1	1	0		1 0 1 0
1	1	1		1 0 0 1

X5	X4	X3	X2	X1	VECTOR D1-D3 (See Fig. 3)
0	0	0	0	0	A A A A
0	0	0	0	1	A C E G
0	0	0	1	0	A B C D
0	0	0	1	1	A D G B
0	0	1	0	0	B B B B
0	0	1	0	1	B D F H
0	0	1	1	0	B C D E
0	0	1	1	1	B E H C
0	1	0	0	0	C C C C
0	1	0	0	1	C E G A
0	1	0	1	0	C D E F
0	1	0	1	1	C F A D
0	1	1	0	0	D D D D
0	1	1	0	1	D F H B
0	1	1	1	0	D E F G
0	1	1	1	1	D G B E
1	0	0	0	0	E E E E
1	0	0	0	1	E G A C
1	0	0	1	0	E F G H
1	0	0	1	1	E H C F
1	0	1	0	0	F F F F
1	0	1	0	1	F H B D
1	0	1	1	0	F G H A
1	0	1	1	1	F A D G
1	1	0	0	0	G G G G
1	1	0	0	1	G A C E
1	1	0	1	0	G H A B
1	1	0	1	1	G B E H
1	1	1	0	0	H H H H
1	1	1	0	1	H B D F
1	1	1	1	0	H A B C
1	1	1	1	1	H C F A

82

FIG. 2-6 - Format III Transfer Function

TIME SLOT	OUTPUT VECTOR D3	D2	D1	SIGN D0
00	X3	X2	X1	X0
01	X7	X6	X5	X4

FIG. 2-7 - Format IV Transfer Function

INPUT WORD

X0	X1	X2	X3	X4	X5	X6	X7
0	0	0	1	1	0	1	0

OUTPUT

TIME SLOT	VECTOR SIGN D3	D2	D1	D0
00	0	0	1	0
01	0	1	0	0
02	0	1	1	1
03	1	0	0	1
04	1	0	1	0
05	1	1	0	0
06	1	1	1	1
07	0	0	0	1

FIG. 2-8 - Example of Encoder Operation, Format II

INPUT WORD

X0	X1	X2	X3	X4	X5	X6	X7
0	0	0	1	1	0	1	0

OUTPUT

TIME SLOT	VECTOR SIGN D3	D2	D1	D0
00	1	0	0	0
01	0	1	0	1

FIG. 2-9 - Example of Encoder Operation, Format IV

3. Encoder Logic Description

3.1 Circuitry Used

The 74LS family of Low Power Schottky TTL circuitry is used to implement the encoder design, except that 74S Schottky TTL circuitry is used to provide additional drive capability for outputs, and in one case as part of a delay circuit.

Although the 74LS and 74S families of circuitry are used, the fan-in and fan-out restrictions of 54LS and 54S circuitry have been adhered to, so that this military temperature range circuitry can be substituted, piecemeal or throughout, without necessitating any design change.

3.2 Logic Conventions

Logical "1" = True = High TTL level
Logical "0" = False = Low TTL level

3.3 Block Diagram

Figure 3-1 is a block diagram of the encoder logic, which consists of the following seven sections:

- Input Terminations and Buffers
- Shift Register
- Time Counter
- Vector Generator
- Sign Generator
- Output Drivers
- Test Circuits

The main signal names used in the logic are shown. In the detailed description of the logic to follow, reference is made to the logic diagram, consisting of five sheets. Figure 3-1 shows the sheet number on which each of the seven sections may be found.

3.4 Circuit Board Layout

The encoder is packaged on a single circuit board; Figure 3-2 shows the layout and the locations of the seven logic sections. The locations of the individual integrated circuits on the circuit board are numbered 1 through 60.

3.5 Logic Diagram

Data/Ware Development, Inc. drawing number LD113010 is a detailed logic diagram of the encoder, to which the following description of operation will refer.

The circuits in the logic diagram have reference designators starting with the letter "U". "U36", for example, means the integrated circuit package at circuit board location 36 (Fig. 3-2). Further, in the detailed descriptions which follow, "U36-6" means the particular circuit (within package U36) having output pin 6, to differentiate it from other circuits in the same package.

Signal names such as "RESET" and "$\overline{\text{LOAD}}$" (where "$\overline{\text{LOAD}}$" is the inverse of "LOAD") are used in the logic diagram and in the following descriptions. A signal name starting with the letter "Q" is the output of a flip-flop or register bit having that same name. For example, flip-flop QT1 has output QT1 and $\overline{\text{QT1}}$.

The 400 KHz Clock is the main clock used in the encoder, and has the signal name "CLK". Data is entered into flip-flops at the rise of CLK (except where specifically noted otherwise).

3.6 Timing Diagrams

Figures 3-3 through 3-6 are timing diagrams for Formats I through IV, respectively, to aid in an understanding of the following detailed descriptions.

3.7 Detailed Description

3.7.1 Input Terminations and Buffers

Sheet 1 of the logic diagram shows the Input Terminations and Buffers.

Four of the input signals are terminated with networks which are the equivalent of a 132-ohm resistor to +3 volts DC. They provide a terminating resistance approximately equal to the characteristic impedance of the twisted pair cables on which these signals are brought to the encoder. The +3 volts is chosen to be compatible with the drive capabilities of the external circuitry.

All the input signals are buffered with inverters, to provide enough drive for the rest of the logic circuitry where the signals are used. Note in particular the signal names used for the interface signals after buffering.

The signals TRUE1 and TRUE2 are used for unused inputs to gates in the rest of the logic. There are two of them simply because of loading restrictions.

3.7.2 Shift Register

The 8-bit Shift Register QA0-QA7 (logic diagram sheet 1) shifts the input data X0-X7 (DATA) into the register at the fall of the Data Bit Clock (the rise of DATCLK). Figures 3-3 through 3-6 depict the timing. QA0 is the input bit.

A complete word (rather than parts of two different words) is available in the Shift Register at the rise of CLK (400 KHz Clock) occurring at the start of time slot T00, and at no other CLK time. It is this time at which the contents of the Shift Register are transferred to the Sign Generator and Vector Generator. At this time input bits X0-X7 are in QA0-QA7 respectively.

In Format IV, an additional transfer is made at the start of time slot T01. There is not an entire word in the Shift Register at this time, but bits X4-X7, which are the desired ones, are then in QA0-QA3, respectively.

3.7.3 Time Counter

The Time Counter (logic diagram sheet 2) controls the timing of the rest of the logic, counting off the time slots T00, T01, etc., as shown in Figures 3-3 through 3-6.

Flip-flops QT0 (least significant bit) through QT3 (most significant bit), Adder U27, and Data Selector U28 make up a loadable and resettable 4-bit binary counter, which, at the rise of CLK, counts if $\overline{\text{SET}}$ is true and RESET is false, sets to 0001 (time slot T01) if $\overline{\text{SET}}$ and RESET are both false, and resets to 0000 (time slot T00) if RESET is true.

Flip-flops QW1-QW2 and NAND gate U26-11 provide the $\overline{\text{SET}}$ signal, which synchronizes the time counter with the Word Clock (WDCLK). $\overline{\text{SET}}$ goes false at the fall of the 400 KHz Clock (rise of $\overline{\text{CLK}}$) next following the rise of the Word Clock (WDCLK); the fall of CLK is used to avoid timing race problems resulting from jitter between the rise of CLK and WDCLK. $\overline{\text{SET}}$ stays false until the next rise of CLK, when the time counter is set to 0001 (T01).

Gates U26-3, -6, -8; inverters U25-2, -4, -6; Data Selector U13-7; and inverter U25-8 provide the RESET and $\overline{\text{RESET}}$ signals, depending on the format ($\overline{\text{FORMX}}$, $\overline{\text{FORMY}}$), as follows:

Format	FORMX	FORMY	Reset at end of:
I	1	1	T15
II	1	0	T07
III	0	1	T03
IV	0	0	T01

Thus the time counter resets to zero (T00) after the proper number of counts for each format.

Data Selector U13-9 provides the $\overline{\text{LOAD}}$ signal, which transfers the contents of the Shift Register to the Sign Generator and Vector Generator. In Formats I, II, and III this happens at the same time as RESET resets the time counter, namely at the end of T15, T07, or T03 (the beginning of T00). In Format IV, $\overline{\text{LOAD}}$ is always false, causing two transfers from the Shift Register for each input word, as previously described.

3.7.4 Vector Generator

The Vector Generator (logic diagram sheet 3) consists of five flip-flops QD1-QD3 and QV1-QV2, Adder U22, and Data Selectors U18-U21.

Inspection of Figures 2-3 through 2-6 reveals that, in Formats I, II, and III, the vector outputs (QD1-QD3) consist of a starting configuration dependent on certain input data bits, followed by repetitively adding a number from 0 to 3 to the starting configuration, this number also being dependent on the input data bits. The number is added modulo-8; for example, adding 3 to 6 results in 1, such as happens when using a 3-bit binary counter.

The starting configuration is loaded into QD1-QD3, and the number by which to count is loaded into QV1-QV2, from Shift Register bits QA1-QA6, at the rise of CLK when $\overline{\text{LOAD}}$ is false. The format ($\overline{\text{FORMX}}$, $\overline{\text{FORMY}}$) controls which Shift Register bits go where.

During adding time ($\overline{\text{LOAD}}$ is true), Adder U22 repetitively adds the contents of QV1-QV2 to the contents of QD1-QD3, placing the result in QD1-QD3. Of course, when QV1-QV2 contain zero, the contents of QD1-QD3 do not change.

In Format IV, Shift Register bits QA1-QA3 are loaded into QD1-QD3 twice per input word. The first time (end of T01, beginning of T00) QA1-QA3 contain input data bits X1-X3; the second time (end

of T00, beginning of T01) QA1-QA3 contain input data bits X5-X7. There is no adding in Format IV, not only because QV1-QV2 contain zero, but because $\overline{\text{LOAD}}$ is always false.

3.7.5 Sign Generator

The Sign Generator is on logic diagram sheet 4, except for flip-flop QD0 (U23-15) and Data Selector U21-12, which are on sheet 3.

Inspection of Figures 2-4 through 2-6 reveals that, in Formats I, II, and III, the sign output consists of an individual bit of the time counter or a particular combination of Exclusive-OR operations of individual bits of the time counter, depending on the input data bits.

As previously mentioned, the sign output when X0 is "1" is the inverse of that when X0 is "0", in Formats I, II, and III; in other words, the bottom half of a sign matrix (Figures 2-4 through 2-6) is the same function of time counter bits as the top half; once this function is generated, an Exclusive-OR of the function with X0 produces both halves of the entire sign matrix.

Inspection of Figures 2-4 through 2-6 reveals also that the top half of the Format II matrix (Figure 2-5) is the same as the upper left-hand corner of the Format I matrix (Figure 2-4). Also, the Format III matrix (Figure 2-6) is a sub-set of the Format II matrix (Figure 2-5), in that the Format III matrix is arrived at by taking every other horizontal row in the top half of the Format II matrix during the first four time slots (the only four, for Format III).

The most significant time counter bit (QT3) is used only in Format I, and the Format I top half (Figure 2-4) may be generated by an Exclusive-OR of the Format II top half (Figure 2-5) with a function consisting of the most significant time counter bit (QT3) ANDed with input data bit X6.

The operation of the Sign Generator can now be explained, referring to logic diagram sheet 4.

Exclusive-OR gates U35-3, -6, -8, -11 and Data Selector U34-6 generate the inverse of the top half of the sign matrix shown in Figure 2-5. Flip-flops QS1-QS3 control which horizontal row of the sign matrix is generated. QS1-QS3 are loaded appropriately with input data bits X1, X2, X6, and X7 from Shift Register bits QA1, QA2, QA6, and QA7 respectively, at the rise of CLK when $\overline{\text{LOAD}}$ is false. Which of the input data bits goes where is controlled through Data Selectors U31-9, U32-7, and U32-9, and depends on the format ($\overline{\text{FORMX}}$, $\overline{\text{FORMY}}$).

In Format I, input data bit X6 is loaded into QS4 from Shift Register bit QA6. NAND gate U30-3 and Exclusive-OR gate U36-3 combine QS4 and time counter bit QT3 appropriately with Data Selector Output U34-6. Exclusive-OR gate U36-3 inverts Data Selector output U34-6 except in Format I when QT3 and QS4 are both true. Since the inverse of the desired function is provided at U34-6, the result is that the desired function is delivered at U36-3. This function is the top half of the sign matrix, in Formats I, II, or III.

In Formats I, II, and III, input data bit X0 is loaded into QD0 (logic diagram sheet 3) from Shift Register Bit QA0. QD0 is Exclusively-OR'd with output U36-3 (sheet 4), yielding the inverse of the desired sign output at U36-6. By appropriately Exclusive-ORing with false (ground) and true (TRUE1), the desired sign output (SIGN) and its inverse ($\overline{\text{SIGN}}$) are delivered at U36-11 and U36-8, respectively.

In Format IV, Shift Register bit QA0 is loaded into QD0 twice per input word. The first time (end of T01, beginning of T00) QA0 contains input data bit X0; the second time (end of T00, beginning of T01) QA0 contains input data bit X4. In this

format (IV), QS1-QS4 and QT3 are all false; thus U36-3 is false, QD0 appears unaltered at U36-6 and at U36-8 ($\overline{SIGN}$), and QD0 appears at U36-11 (SIGN), as desired.

3.7.6 Output Drivers

Output Drivers U8-3, -6, -8, -11 (logic diagram sheet 3) are inverting drivers; thus the inverses of the desired output signals are used at the driver inputs. $\overline{QD1}$, $\overline{QD2}$, and $\overline{QD3}$ from the Vector Generator result in outputs D1, D2, and D3 respectively, and $\overline{SIGN}$ from the Sign Generator results in output D0.

3.7.7 Test Circuits

The Test Circuits are provided solely for the purpose of testing the encoder. When the encoder is not being tested, the integrated circuit packages which are used exclusively in the Test Circuits may be removed. These packages are U39 through U46. Packages U24 and U30 are also used in the Test Circuits, but they are shared with the Vector Generator (U24) and Sign Generator (U30), so must always remain in place.

The Test Circuits are on logic diagram sheet 5, except for flip-flop QTEST (U24-10), which is on sheet 3.

The Test Circuits produce pulses LP1 and LP2 (Figures 3-3 through 3-6). LP1 is used by external circuitry to sample test latch register QL0-QL7 (input data to encoder), and LP2 is used to sample SIGN and QD0-QD3 (output data from encoder).

QTEST (logic diagram sheet 3) is true during T00, and is gated with LP2 at U30-8 (sheet 5) to produce LP1 at U41-6. In addition, the rising edge of QTEST is used to load test latch register QL0-QL7.

LP2 is produced from CLK as follows: U41-2 provides adequate drive for inputs U42-1&2; U42-3 and RC network U43 provide CLKD (CLK delayed, with slow rise and fall times) at U30-13. U30-11

is the inverse of LP2. LP2 appears at U41-10, with adequate drive for inputs U42-12&13, and its equivalent appears at U41-8 and at U30-10, where it is gated with Q"EST, resulting in LP1 at U41-6.

In addition to the signals previously mentioned, $\overline{\text{WDCLK}}$ is inverted at U41-4, resulting in the logical equivalent of WDCLK at inputs U42-4&5.

Connectors J52, J54, and J56 provide signals externally for test purposes. These connectors are simply the integrated circuit sockets at locations 52, 54, and 56 of the circuit board (Figure 3-2). J54 and J56 provide outputs of high drive capability through inverting drivers U42-6, -8, -11, U44, U45, and U46. Connector J52 carries some internal logic signals which should be connected only to an oscilloscope or other high-impedance device.

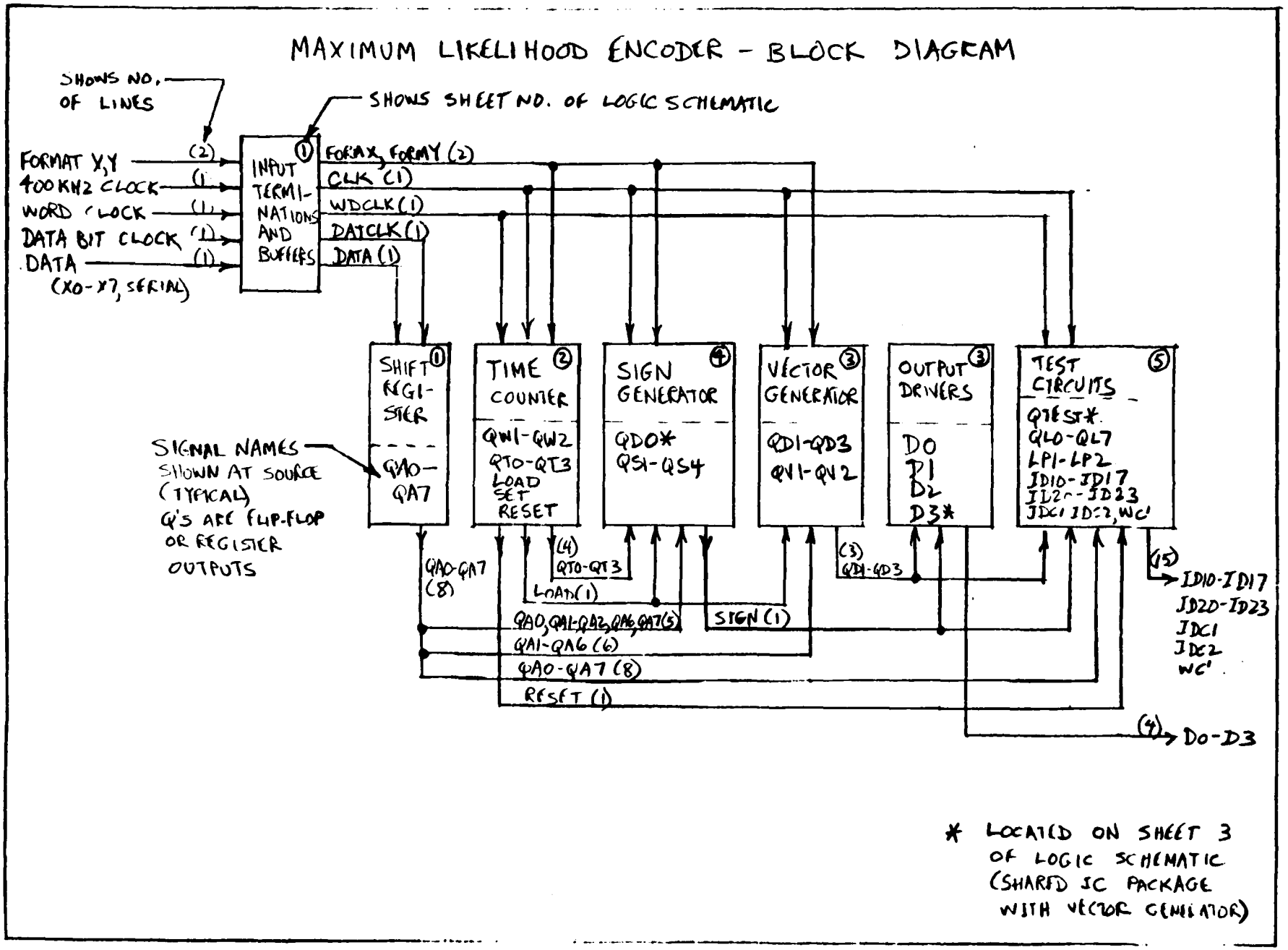
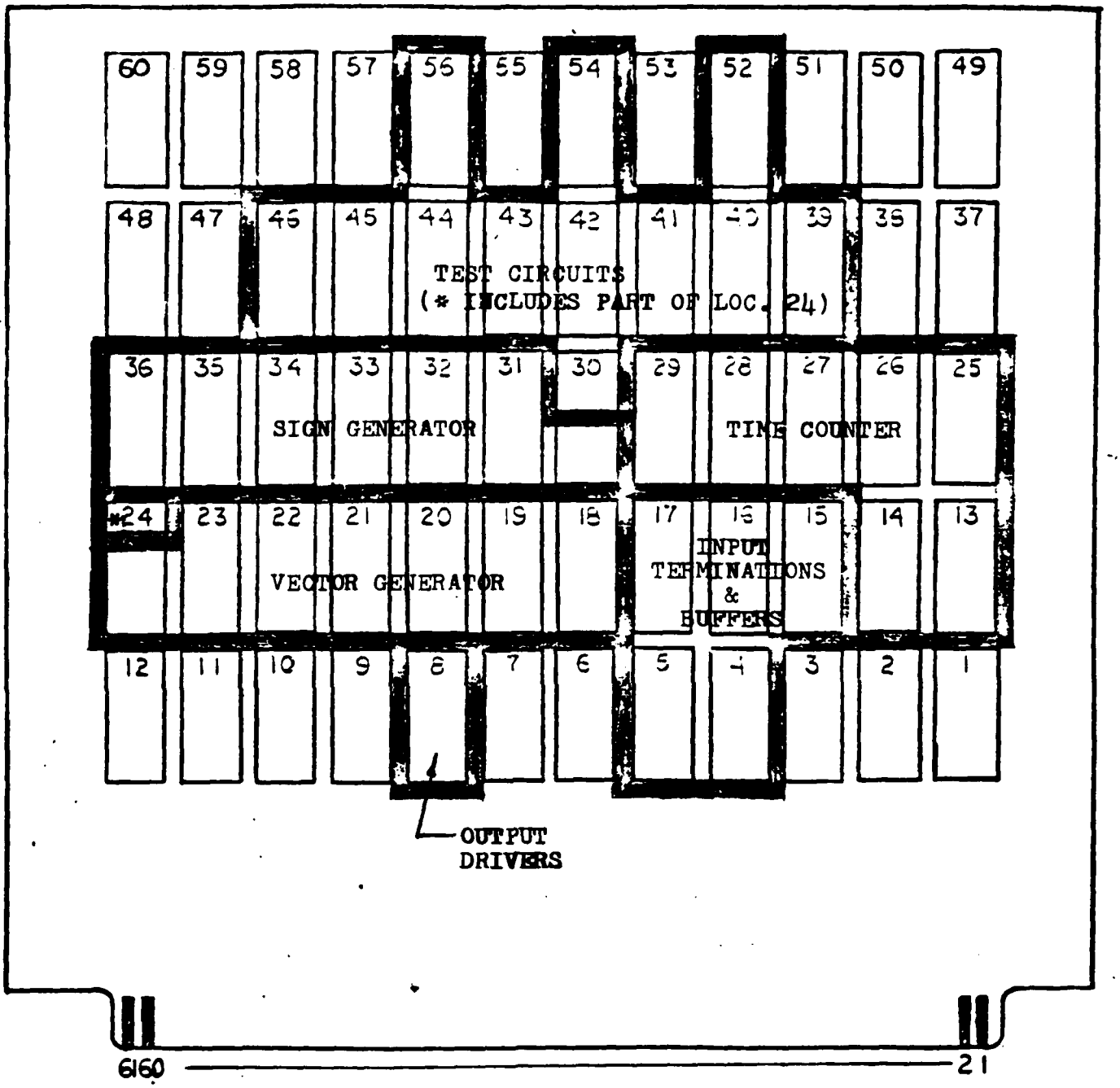


FIG. 3-1 - ENCODER LOGIC BLOCK DIAGRAM



Component Side Shown

FIG. 3-2 - CIRCUIT BOARD LAYOUT

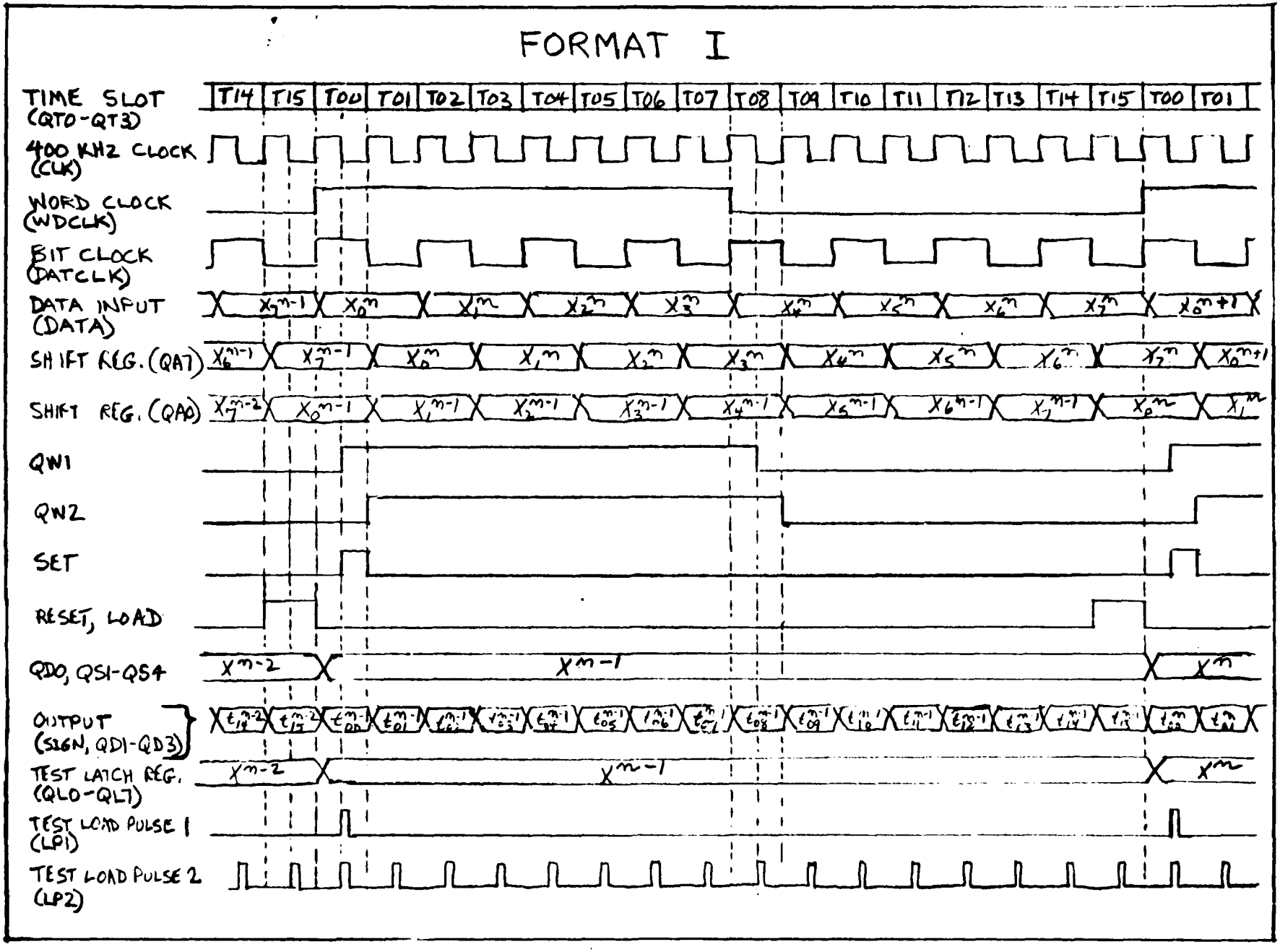


FIG. 3-3 - FORMAT I TIMING

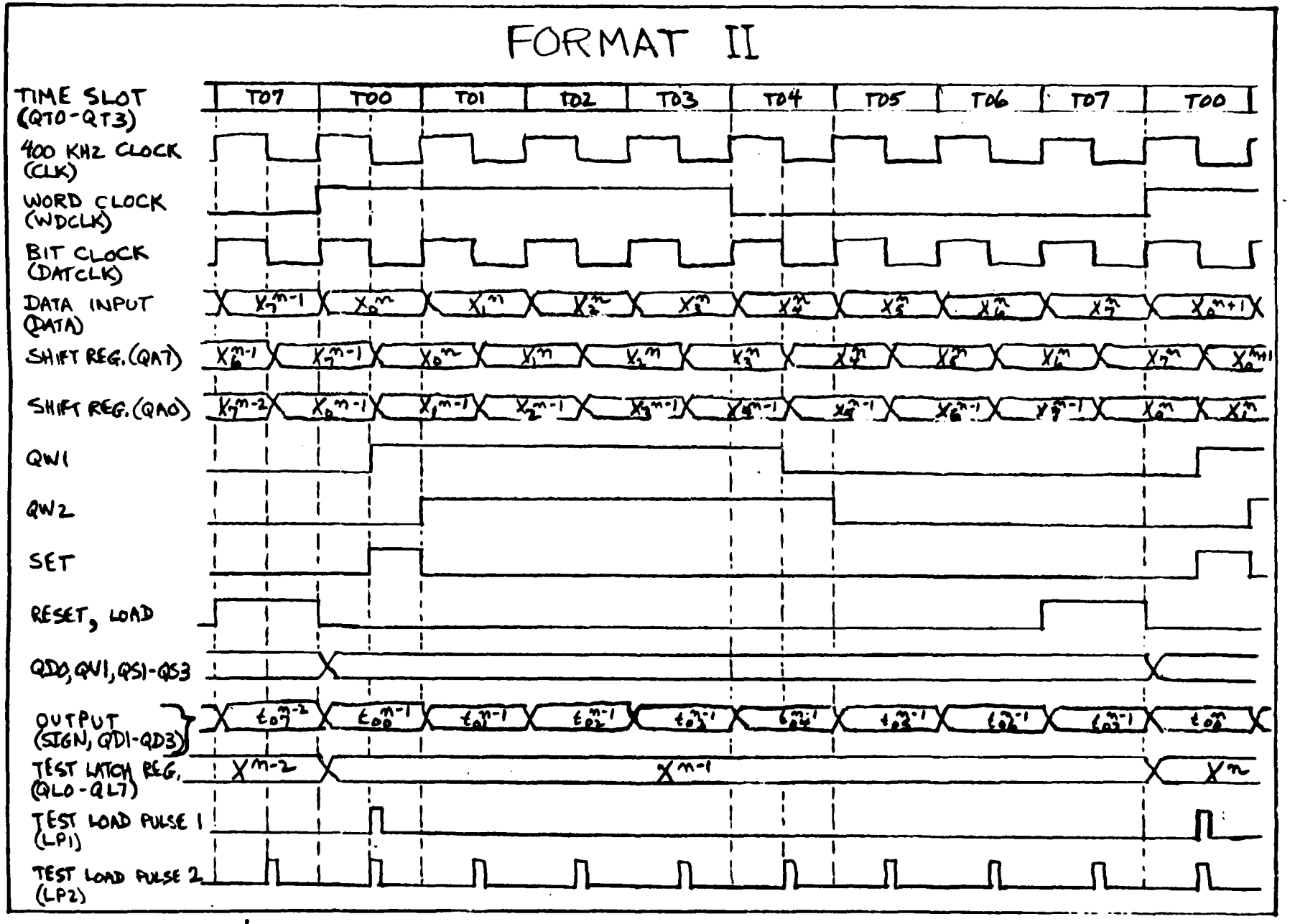


FIG. 3-4- FORMAT II TIMING

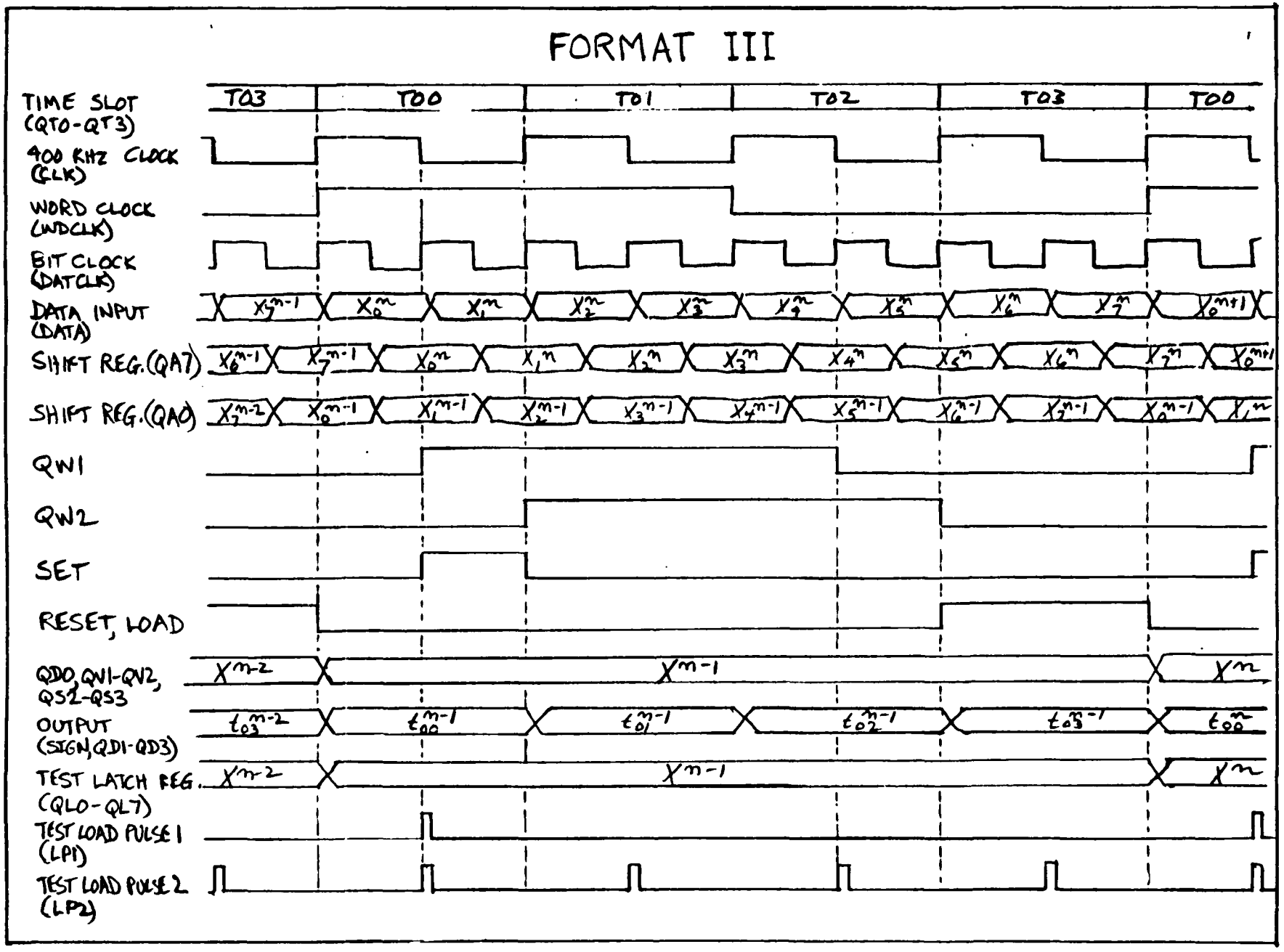


FIG. 3-5 - FORMAT III TIMING

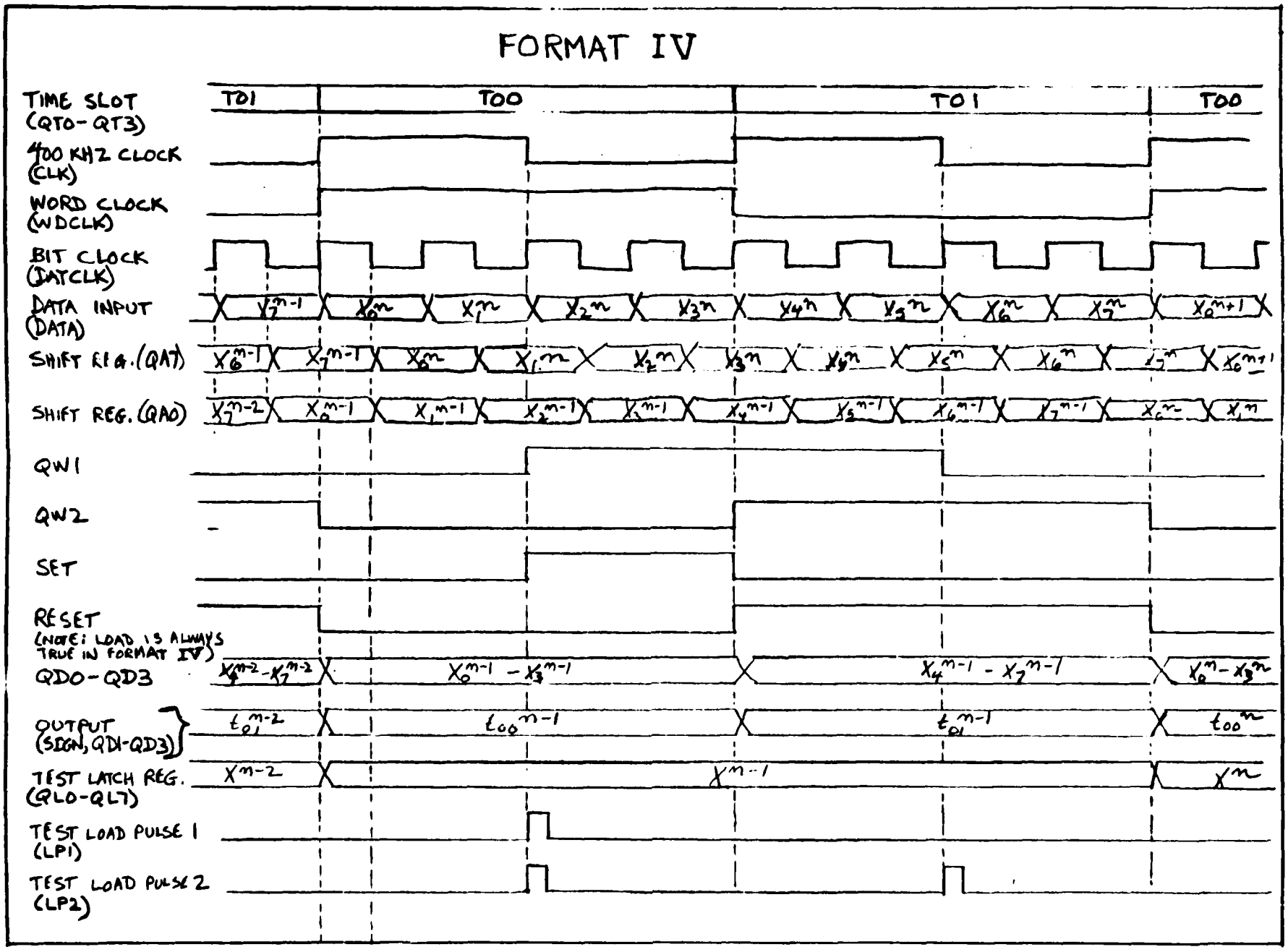


FIG. 3-6 - FORMAT IV TIMING

4. Decoder Logic Design

4.1 General

The decoder is a soft-decision, maximum-likelihood type which accepts data from the Harris video modem in any one of four formats, as shown in Table 1-1.

The decoder receives encoded data as 8 3-bit words at 400 KHz and produces video output signals at 200, 400, and 800 K bits/sec. These output rates correspond, respectively, to data encoded in Formats I, II, and III. A further requirement is that the decoder accept a fourth data format. Format IV data is non-encoded and the decoder must pass the identity and sign of the largest filter output (A to H) directly to the video output interface.

Since the input data stream to the encoder is blocked into 8-bit characters which are encoded, the decoder must select the most likely output from among 256 possible ones. The decoder systematically tries each of the 256 correlations on the received compound vector and selects the best fit.

4.2 Decoder Organization

The decoder interfaces to both the Harris Modem and the video output terminal. The Harris Modem provides to the decoder in parallel digital representations of matched filters A to H responses to the received data. The decoder will group the filter outputs to form compound vectors that will be correlated, using Fast Walsh Transform techniques, with the elements of a Reed-Muller sign matrix. (See Table 1-1). The maximum likelihood vector will be selected from the correlated resultants and the associated 8-bits of decoded data will be output after a three-word delay to the video terminals at a rate indicated by the operating data format.

The decoder design is logically divided into three sections as shown in Figure 4-1. The Correlator and Selector sections comprise the data handling and processing functions of the decoder and the Control section provides the necessary switching functions, memory addressing etc.

4.3 Decoder Correlator

The main elements of the correlator section are RAM's, ADDERS and Data Selectors. The RAM's serve as storage for initial values and intermediate results. The ADDERS perform the Fast Walsh Transform calculations to generate the sign patterns of Table 1-1 and the Data Selectors perform the necessary data routing functions. Since the largest compound vector (in Format I) consists of 16 base vectors, there is a requirement for four "levels" of adders to perform addition and subtraction on the filter outputs. Formats II and III require three levels and two levels, respectively. These adder levels are also referred to as iterations. (Refer to Figures 4-2 to 4-5).

Data is input to the decoder via three 8:1 data selectors and stored in memories M_{00} to M_{03}. During each 2.5 usec period digital values for filters A to H are written into one of the four M_{00} to M_{03} memories. When four sets of filter values have been input the data is read out in parallel (An...An+3, Bn...Bn+3 etc.) to the ADDER section. (Actually both read and write occur during each 2.5 usec since there is a constant data flow into and out of the decode system. The memories, therefore, are used in a ping pong fashion to accomodate for the continuous data flow). Note that the filter outputs are processed in groups of four.

The decoder design assumes that the input data will be a 3-bit one's complement representation of the A through H filter outputs.

LATCH 1 is used as a holding register between M_{00}-M_{03} and the first and second iteration adders. The parallel data from $M_{00}\cdots M_{03}$ through LATCH 1, is output to ten ADDERS (Figure 4-3) where two iterations of a Fast Walsh Transform (FWT) are performed. The resulting values held in LATCH 2 are sent to the "select" section if the system is operating in Format III and are routed via three dual 4:1 selectors (SELECTOR 1) to additional processing circuitry if the system is operating in Formats I or II. Tables 4-1 to 4-4 provide a means of identifying the vectors that are generated at the various steps of the FWT process for each of the three data formats.

The RAM's ADDERS and data selectors shown in Figures 4-4 and 4-5 provide the additional processing necessary to complete the correlation process for data Formats I and II. The correlation is completed for Format II by the following steps.

1. Vectors $A_0''\ldots A_3''\ldots H_0''\ldots H_3''$ calculated in iterations 1 and 2 are stored in M_{10}.
2. As $A_4''\ldots A_7''\ldots H_4''\ldots H_3''$ are created they are output to the second set of ALU's via data selectors and latches.
3. Simultaneously with step 2 the stored vectors in M_{10} are read out to the ALU's, hence, completing the final FWT calculation for Format II.

There are two additional iterations required to complete the correlation of Format I data. Beginning with the iteration 1 and 2 data values the step by step process is

1. Vectors $A_0''\ldots A_3''\ldots H_0''\ldots H_3''$ are written into M_{10}
2. Vectors $A_4''\ldots A_7''\ldots H_4''\ldots H_7''$ are written into M_{11}
3. As vectors $A_8''\ldots A_{11}''\ldots H_8''\ldots H_{11}''$ are created they are routed to the ADDERS.
4. Simultaneously with step 3 vectors $A_0''\ldots A_3''\ldots H_0''\ldots H_3''$ are read out of M_{11} to the ADDERS and summed and differenced with vectors $A_8''\ldots A_{11}''\ldots H_8''\ldots H_{11}''$

FORMAT I NOTATION

ITER 1 & 2

$$A''_0 = A_0 + A_1 + A_2 + A_3$$
$$A''_1 = A_0 + A_1 - A_2 - A_3$$
$$A''_2 = A_0 - A_1 + A_2 - A_3$$
$$A''_3 = A_0 - A_1 - A_2 + A_3$$

$$A''_4 = A_4 + A_5 + A_6 + A_7$$
$$A''_5 = A_4 + A_5 - A_6 - A_7$$
$$A''_6 = A_4 - A_5 + A_6 - A_7$$
$$A''_7 = A_4 - A_5 - A_6 + A_7$$

$$A''_8 = A_8 + A_9 + A_{10} + A_{11}$$
$$A''_9 = A_8 + A_9 - A_{10} - A_{11}$$
$$A''_{10} = A_8 - A_9 + A_{10} - A_{11}$$
$$A''_{11} = A_8 - A_9 - A_{10} + A_{11}$$

$$A''_{12} = A_{12} + A_{13} + A_{14} + A_{15}$$
$$A''_{13} = A_{12} + A_{13} - A_{14} - A_{15}$$
$$A''_{14} = A_{12} - A_{13} + A_{14} - A_{15}$$
$$A''_{15} = A_{12} - A_{13} - A_{14} + A_{15}$$

ITER 3

$$A^3_0 = A''_0 + A''_8$$
$$A^3_1 = A''_1 + A''_9$$
$$A^3_2 = A''_2 + A''_{10}$$
$$A^3_3 = A''_3 + A''_{11}$$
$$A^3_4 = A''_4 + A''_{12}$$
$$A^3_5 = A''_5 + A''_{13}$$
$$A^3_6 = A''_6 + A''_{14}$$
$$A^3_7 = A''_7 + A''_{15}$$
$$A^3_8 = A''_0 - A''_8$$
$$A^3_9 = A''_1 - A''_9$$
$$A^3_{10} = A''_2 - A''_{10}$$
$$A^3_{11} = A''_3 - A''_{11}$$
$$A^3_{12} = A''_4 - A''_{12}$$
$$A^3_{13} = A''_5 - A''_{13}$$
$$A^3_{14} = A''_6 - A''_{14}$$
$$A^3_{15} = A''_7 - A''_{15}$$

ALSO $B^3_0 \cdots H^3_{15}$

ITER 4

$$A^4_0 = A^3_0 + A^3_4$$
$$A^4_1 = A^3_0 - A^3_4$$
$$A^4_2 = A^3_1 + A^3_5$$
$$A^4_3 = A^3_1 - A^3_5$$
$$A^4_4 = A^3_2 + A^3_6$$
$$A^4_5 = A^3_2 - A^3_6$$
$$A^4_6 = A^3_3 + A^3_7$$
$$A^4_7 = A^3_3 - A^3_7$$
$$A^4_8 = A^3_8 + A^3_{12}$$
$$A^4_9 = A^3_8 - A^3_{12}$$
$$A^4_{10} = A^3_9 + A^3_{13}$$
$$A^4_{11} = A^3_9 - A^3_{13}$$
$$A^4_{12} = A^3_{10} + A^3_{14}$$
$$A^4_{13} = A^3_{10} - A^3_{14}$$
$$A^4_{14} = A^3_{11} + A^3_{15}$$
$$A^4_{15} = A^3_{11} - A^3_{15}$$

ALSO $B^4_0 \cdots H^4_{15}$

FORMAT II
ITER 1 & 2

$A''_0 \quad A_0 + A_1 + A_2 + A_3$
$A''_1 \quad A_0 + A_1 - A_2 - A_3$
$A''_2 \quad A_0 - A_1 + A_2 - A_3$
$A''_3 \quad A_0 - A_1 - A_2 + A_3$

$A''_4 \quad A_4 + A_5 + A_6 + A_7$
$A''_5 \quad A_4 + A_5 - A_6 - A_7$
$A''_6 \quad A_4 - A_5 + A_6 - A_7$
$A''_7 \quad A_4 - A_5 - A_6 + A_7$

Also GENERATE

B''_0	to B''_3	B''_4	to B''_7
C''_0	C''_3	C''_4	to C''_7
D''_0	D''_3	D''_4	to D''_7
E''_0	E''_3	E''_4	to E''_7
F''_0	F''_3	F''_4	to F''_7
a''_0	a''_3	a''_4	to a''_7
b''_0	b''_3	b''_4	to b''_7
c''_0	c''_3	c''_4	to c''_7
d''_0	d''_3	d''_4	to d''_7
e''_0	e''_3	e''_4	to e''_7
f''_0	f''_3	f''_4	to f''_7
g''_0	g''_3	g''_4	to g''_7
h''_0	h''_3	h''_4	to h''_7

TABLE 4-2

FORMAT II
ITER 3.

$$A_0^3 = A_0'' + A_4'' \qquad A_4^3 = A_2'' + A_6''$$
$$A_1^3 = A_0'' - A_4'' \qquad A_5^3 = A_2'' - A_6''$$
$$A_2^3 = A_1'' + A_5'' \qquad A_6^3 = A_3'' + A_7''$$
$$A_3^3 = A_1'' - A_6'' \qquad A_7^3 = A_3'' - A_7''$$

ALSO GENERATE

B_0^3 to B_7^3
C_0^3 C_7^3
D_0^3 D_7^3
E_0^3 E_7^3
F_0^3 F_7^3
G_0^3 G_7^3
H_0^3 H_7^3
a_0^3 a_7^3
b_0^3 b_7^3
c_0^3 c_7^3
d_0^3 d_7^3
e_0^3 e_7^3
f_0^3 f_7^3
g_0^3 g_7^3
j_0^3 h_7^3

FORMAT III
ITER 1 & 2

$$A''_0 = A_0 + A_1 + A_2 + A_3$$
$$A''_1 = A_0 + A_1 - A_2 - A_3$$
$$A''_2 = A_0 - A_1 + A_2 - A_3$$
$$A''_3 = A_0 - A_1 - A_2 + A_3$$

ALSO GENERATE

B''_0 to B''_3
C''_0 C''_3
D''_0 D''_3
E''_0 E''_3
F''_0 F''_3
G''_0 G''_3
H''_0 H''_3

a''_0 to a''_3
b''_0 b''_3
c''_0 c''_3
d''_0 d''_3
e''_0 e''_3
f''_0 f''_3
g''_0 g''_3
h''_0 h''_3

α''_0 to α''_3
β''_0 β''_3
γ''_0 γ''_3
δ''_0 δ''_3
ϵ''_0 ϵ''_3
ζ''_0 ζ''_3
η''_0 η''_3
θ''_0 θ''_3

ι''_0 to ι''_3
κ''_0 κ''_3
λ''_0 λ''_3
μ''_0 μ''_3
ν''_0 ν''_3
ξ''_0 ξ''_3
o''_0 o''_3
π''_0 π''_3

TABLE 4-4

5. New values are then stored in M_{10} and M_{12} and the old $A''_0 \ldots A'' \ldots H''_0 \ldots H''_3$ are replaced by $A^3_0 \ldots A^3_3 \ldots H^3_0 \ldots H^3_3$
6. This process is repeated as vectors $A''_{12} \ldots A''_{15} \ldots H''_{12} \ldots H''_{15}$ are created for memories M_{11} and M_{13}. Steps 3-6 comprise the iteration 3 calculations.
7. Iteration 4 is completed as new vectors $A''_0 \ldots A''_3 \ldots H''_0 \ldots H''_3$ and $A''_4 \ldots A''_7 \ldots H''_4 \ldots H''_7$ are created. As $A''_0 \ldots A''_3 \ldots H''_0 \ldots H''_3$ are created memories M_{10_4} and M_{11} are read out to the ADDERS to form vectors $A^4_0 \ldots A^4_7 \ldots H^4_0 \ldots H^4_7$. Vectors $A''_0 \ldots A''_3 \ldots H''_0 \ldots H''_3$ replace $A^3_0 \ldots A^3_3 \ldots H^4_0 \ldots H^4_3$.
8. Similarly as $A''_4 \ldots A''_3 \ldots H''_0 \ldots H''_3$ are created memories M_{12} and M_{13_4} are read out to the ADDERS to form vectors $A^4_8 \ldots A^4_{15} \ldots H^4_8 \ldots H^4_{15}$, thus completing iteration 4.

Note that it is necessary to perform iterations 1 and 2 in separate adders in order to gain the speed advantage required by data Format III. In Formats I and II, when performing iterations 3 and 4 however, it is possible to use an intermediate store technique, hence realizing a considerable savings in ADDERS (16 ADDERS would have been required to perform iterations 3 and 4 in a similar way to iterations 1 and 2).

4.4 Decoder Selector

The final correlated values for the three formats are output in a fixed, predetermined order to the selector portion which will choose the largest absolute value as the "most likely". The order is used to identify the vector corresponding to the maximum.

The select section (Figures 4-5 and 4-6) are composed of input circuits that perform an absolute value calculation, three levels of magnitude and data select circuits and a vector identification circuit.

The operation of the select circuits is similar for all three data formats. However, an additional level of compare and select

is required for Format III data since four values are input instead of the two values in Formats I or II. Each level of "compare and select" gates the largest input to the next level. At the final stage the largest of the input values is compared with the previous "largest" value. If the new value is largest it is stored for future comparisons. Simultaneously, with the storage of the new "largest" value the sign of the value, the settings of the data selectors, and the counter that identifies the input vector set are stored. When the final value, for any particular frame, has been compared, the sign, count and selector settings will be output yielding the desired decoded data.

4.5 Decoder Control Unit

The purpose of the control unit is to sequence the selectors, memories, and latches during the processing. The control section for the decoder is shown in Figure 4-7. A special circuit takes the 12.8 MHz clock and generates 256 time periods for decoder control. During each time period consisting of two 12.8 MHz clocks a new operation is performed.

The 512 Counter (Figure 4-7) counts down the 12.8 MHz clock. The counter's 8 most significant bits are further processed into control signals, yielding 256 states.

The 512 Counter is synchronized by the Sync Control section. The Sync Control section upon the arrival of a word clock from the modem, checks the 512 counter's states. If the counter is out of step a resync signal is generated to hold the counter until the next word clock. With the arrival of the next word clock the resync is released allowing the counter to start at the proper count.

The State Generator decodes the 256 states into major and minor states. There are a possible 16 major states, and each major state can be further broken into 16 possible minor states.

Actually only 4 major states and 4 of their minor states are decoded for use by the control logic.

The controller sets up to perform an action in the decoder one time period before the action is required. At the beginning of a time period the control signals are frozen by the control latch. Thus the control latch allows time to determine the next operation to be performed.

The Combinational Control section provides most of the necessary control signals. After one of the counter's 256 states has been established as an operation to be performed by the decoder, the Combinational Control section determines the state and format and generates the appropriate control signal.

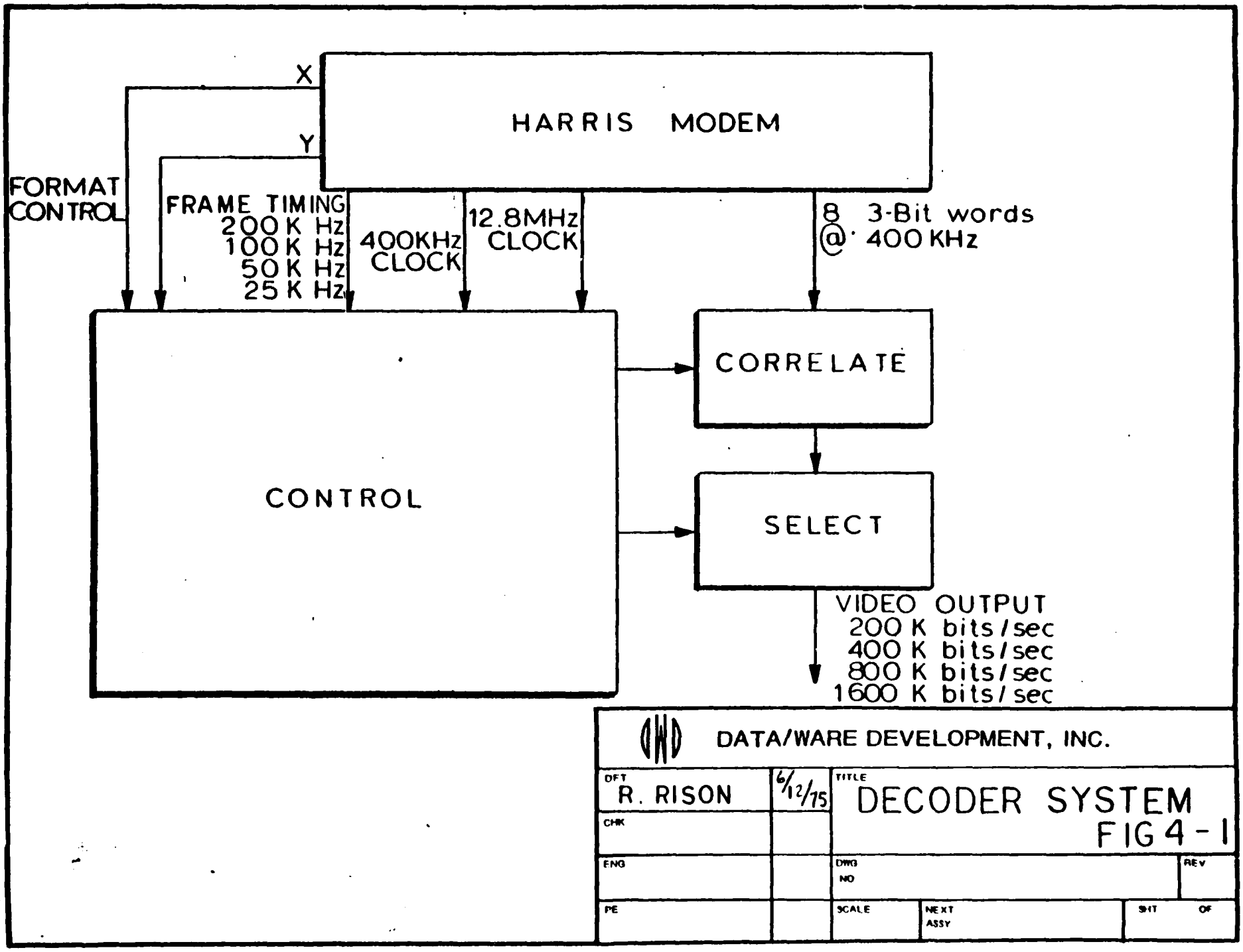
In order to simplify the addressing of memory 1, memory 0's addressing is not in an obvious order. Thus a ROM Address and Control unit is used to hold the addressing for memory 0. This addressing sequence stores and reads the input filter values in an order such that further operation of the decoder can be easily controlled by sequential logic. Bits not used in the ROM for memory 0 addressing are used for control of selector 3 (Figure 4-4).

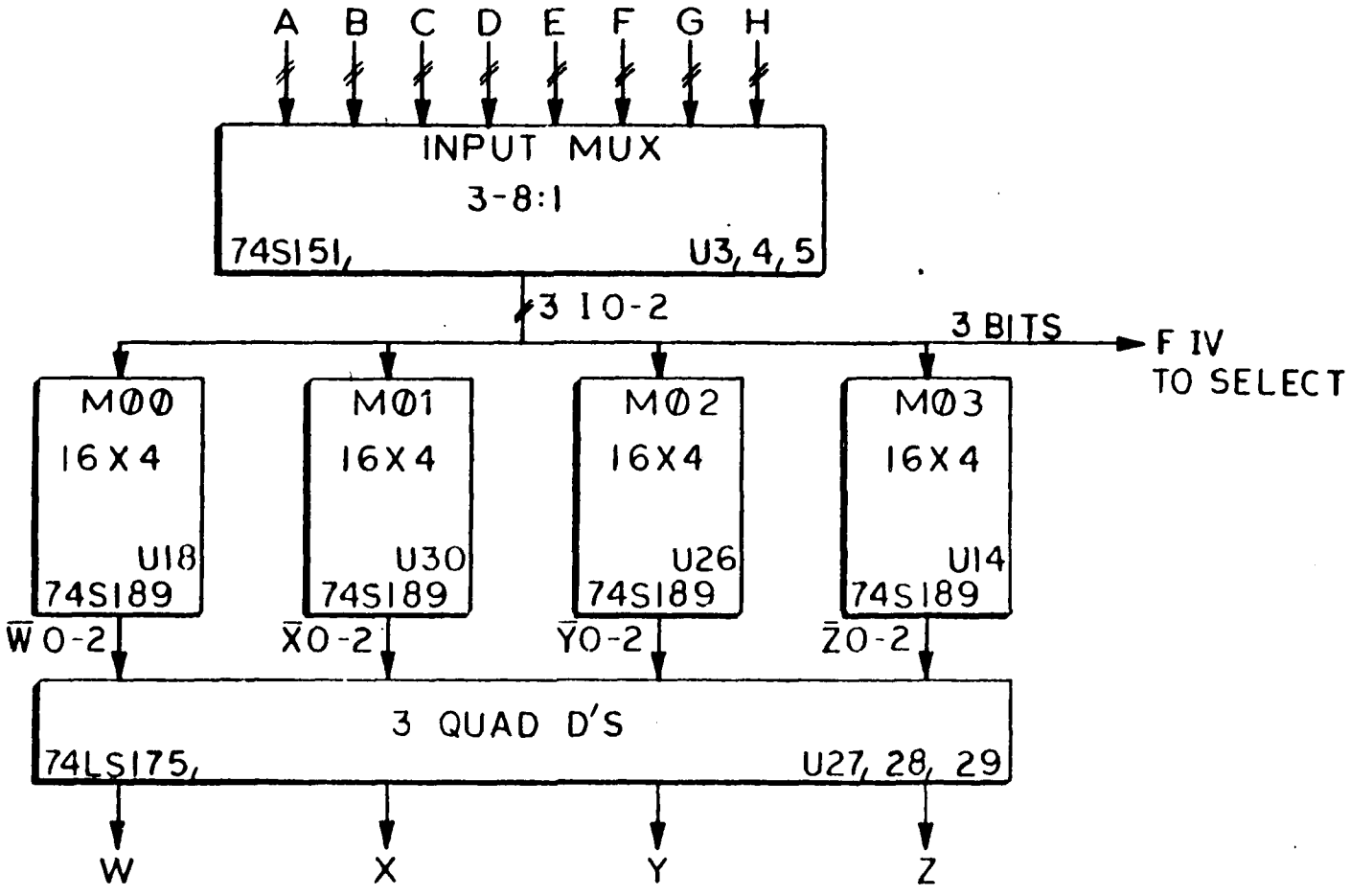
Memory 1 addressing is a simple count. Control of this addressing sequence is performed by a counter circuit adjusted for the specific format by the use of a multiplexer.

The vector counter will identify the actual data to be output. At the final compare of the correlated values the vector counter is incremented. If the new value is greater than the "last greatest" value, the new value will be stored as the "last greatest" value and the contents of the vector counter will be updated. After all correlations have been made and the largest value selected, the 8-bit identification of this value will be output to the TV system as the decoded compound vector.

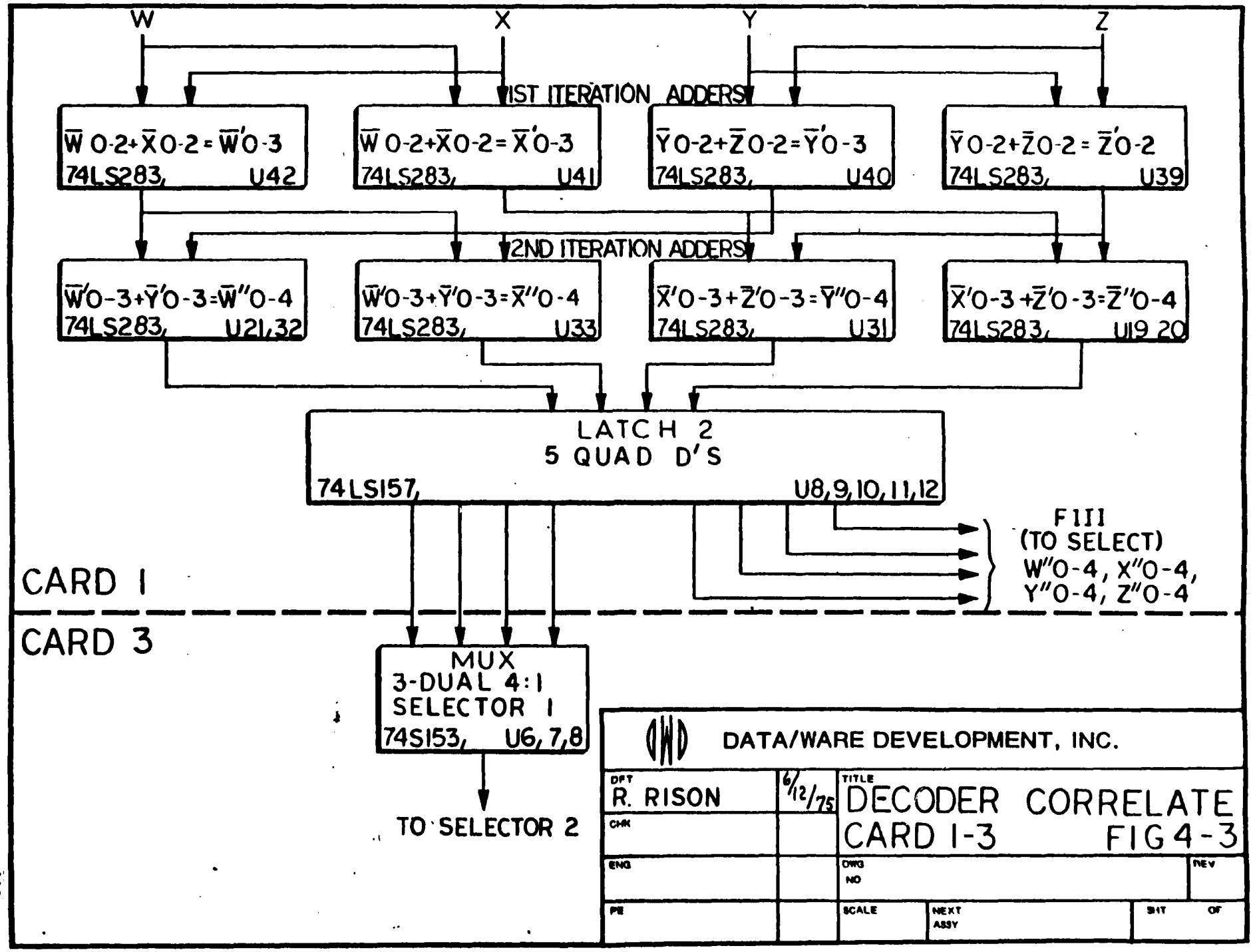
The decoder control section decomposes the processing of a given format into 256 operations. The 256 operations covers one input word in Format I, two words in Format II, four words in Format III and eight words in Format IV. Each operation is set up during the preceding time period and latched in the control latch at the beginning of its time period. Most control functions are performed using conventional control logic.

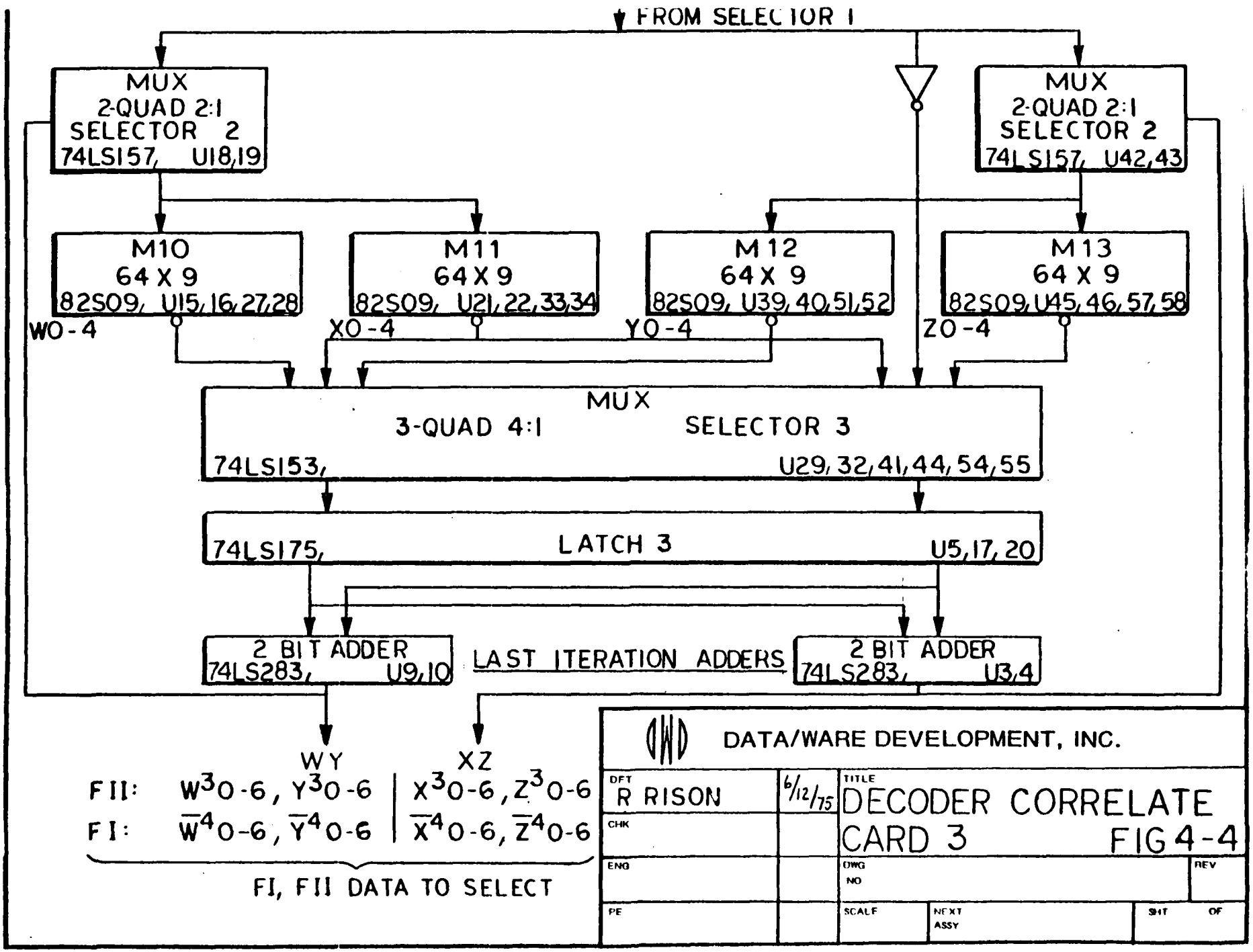
Most of the controller's combinational control is located on card 2 along with the counter, state generator, sync control and memory 1 address and control. The ROM address and control is located with memory 0 on card 2. The control latch is distributed over the three cards of the decoder. Each latch is located so as to be as close as possible to the device it controls.

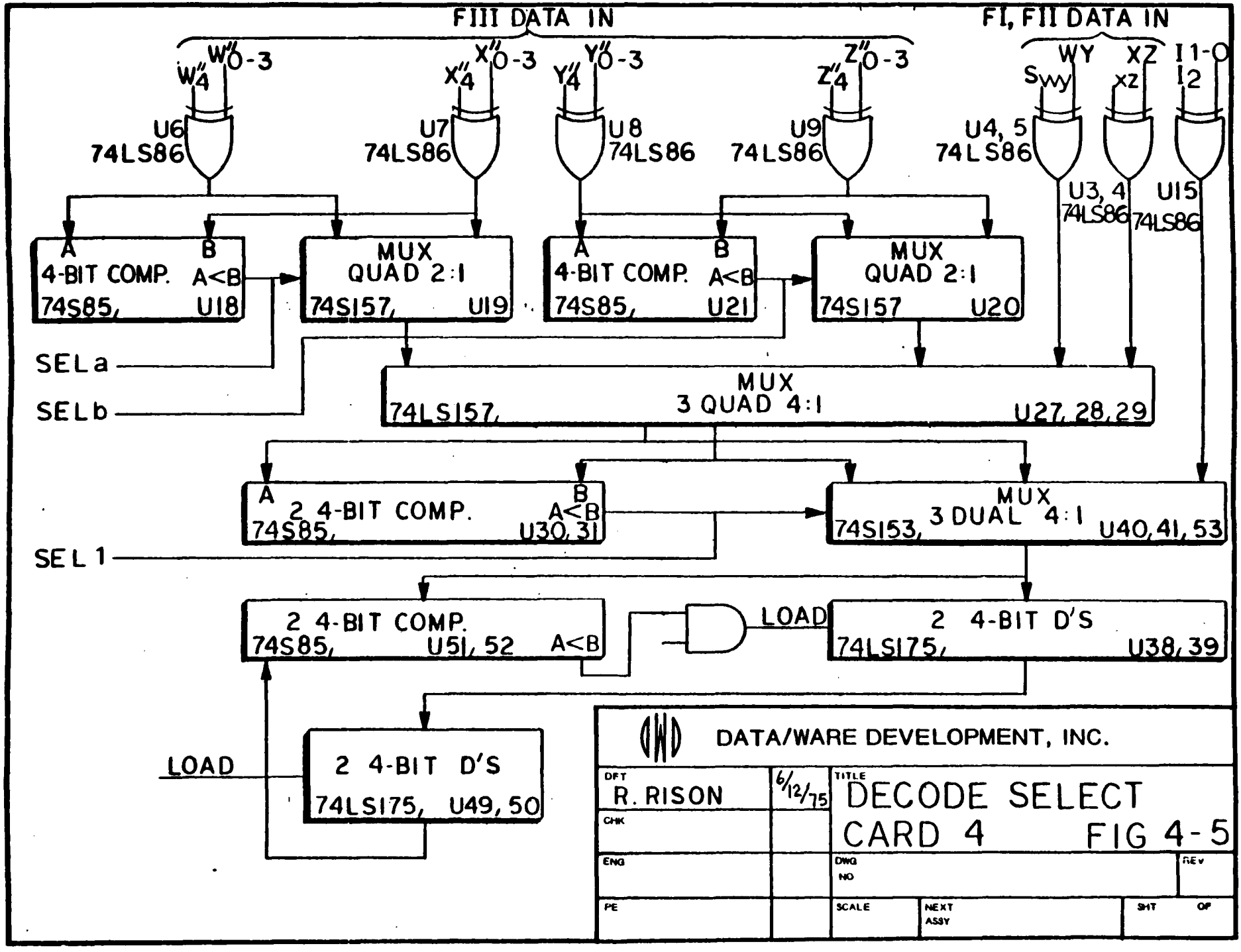

X
Y
HARRIS MODEM
FORMAT CONTROL
FRAME TIMING
200 K Hz
100 K Hz
50 K Hz
25 K Hz
400KHz CLOCK
12.8MHz CLOCK
8 3-Bit words @ 400 KHz
CONTROL
CORRELATE
SELECT
VIDEO OUTPUT
200 K bits/sec
400 K bits/sec
800 K bits/sec
1600 K bits/sec
DATA/WARE DEVELOPMENT, INC.
DFT R. RISON
6/12/75
TITLE
DECODER SYSTEM
FIG 4-1
CHK
ENG
DWG NO
REV
PE
SCALE
NEXT ASSY
SHT
OF

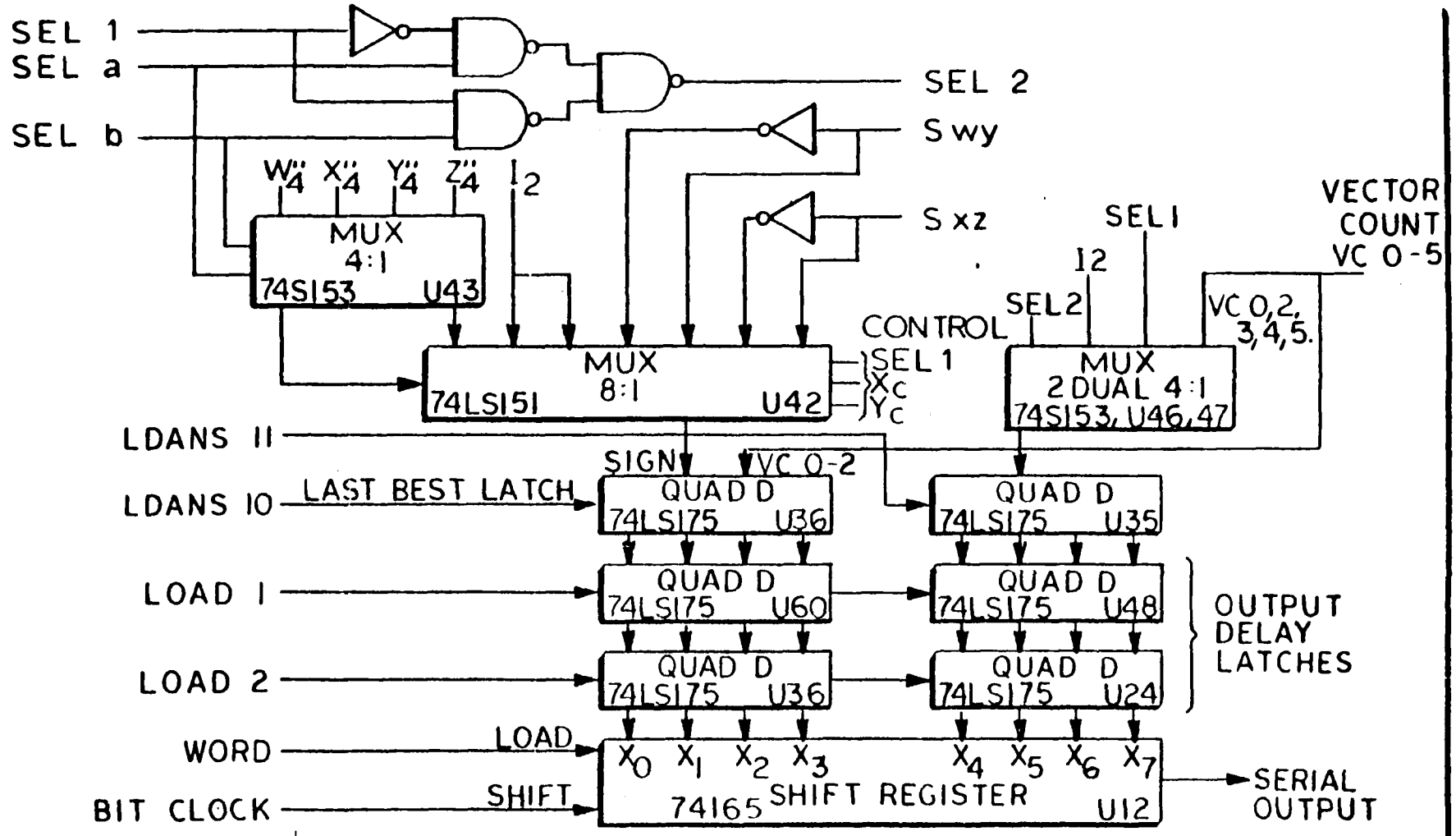


DWD DATA/WARE DEVELOPMENT, INC.			
DFT R. RISON	6/12/75	TITLE DECODER CORRELATE CARD I	FIG4-2
CHK			
ENG		DWG NO	REV
PE		SCALE / NEXT ASSY	SHT OF


W
X
Y
Z
1ST ITERATION ADDERS
W̄ 0-2+X̄0-2 = W̄'0-3
74LS283, U42
W̄ 0-2+X̄0-2 = X̄'0-3
74LS283, U41
Ȳ0-2+Z̄0-2 = Ȳ'0-3
74LS283, U40
Ȳ0-2+Z̄0-2 = Z̄'0-2
74LS283, U39
2ND ITERATION ADDERS
W̄'0-3+Ȳ'0-3 = W̄''0-4
74LS283, U21,32
W̄'0-3+Ȳ'0-3 = X̄''0-4
74LS283, U33
X̄'0-3+Z̄'0-3 = Ȳ''0-4
74LS283, U31
X̄'0-3+Z̄'0-3 = Z̄''0-4
74LS283, U19 20
LATCH 2
5 QUAD D'S
74LS157, U8,9,10,11,12
F111
(TO SELECT)
W''0-4, X''0-4,
Y''0-4, Z''0-4
CARD 1
CARD 3
MUX
3-DUAL 4:1
SELECTOR 1
74S153, U6,7,8
TO SELECTOR 2
DATA/WARE DEVELOPMENT, INC.
DFT R. RISON
6/12/75
CHK
ENG
PE
TITLE
DECODER CORRELATE
CARD 1-3 FIG 4-3
DWG NO
REV
SCALE
NEXT ASSY
SHT OF


FROM SELECTOR 1
MUX
2-QUAD 2:1
SELECTOR 2
74LS157, U18,19
MUX
2-QUAD 2:1
SELECTOR 2
74LS157, U42,43
M10
64 X 9
82S09, U15,16,27,28
M11
64 X 9
82S09, U21,22,33,34
M12
64 X 9
82S09, U39,40,51,52
M13
64 X 9
82S09, U45,46,57,58
W0-4
X0-4
Y0-4
Z0-4
MUX
3-QUAD 4:1 SELECTOR 3
74LS153, U29,32,41,44,54,55
74LS175, LATCH 3 U5,17,20
2 BIT ADDER
74LS283, U9,10
LAST ITERATION ADDERS
2 BIT ADDER
74LS283, U3,4
WY
XZ
FII: W³0-6, Y³0-6 | X³0-6, Z³0-6
FI: W̄⁴0-6, Ȳ⁴0-6 | X̄⁴0-6, Z̄⁴0-6
FI, FII DATA TO SELECT
DATA/WARE DEVELOPMENT, INC.
DFT R RISON
6/12/75
CHK
ENG
PE
TITLE
DECODER CORRELATE
CARD 3 FIG 4-4
DWG NO
REV
SCALE
NEXT ASSY
SHT OF


FIII DATA IN
FI, FII DATA IN
W"4
W"0-3
X"4
X"0-3
Y"4
Y"0-3
Z"4
Z"0-3
WY
XZ
I1-0
I2
Swy
xz
U6
74LS86
U7
74LS86
U8
74LS86
U9
74LS86
U4, 5
74LS86
U3, 4
74LS86
U15
74LS86
A
B
4-BIT COMP.
A<B
74S85, U18
MUX
QUAD 2:1
74S157, U19
A
B
4-BIT COMP.
A<B
74S85, U21
MUX
QUAD 2:1
74S157 U20
SELa
SELb
MUX
3 QUAD 4:1
74LS157, U27, 28, 29
A
B
2 4-BIT COMP.
A<B
74S85, U30, 31
MUX
3 DUAL 4:1
74S153, U40, 41, 53
SEL 1
2 4-BIT COMP.
74S85, U51, 52 A<B
LOAD
2 4-BIT D'S
74LS175, U38, 39
LOAD
2 4-BIT D'S
74LS175, U49, 50
DATA/WARE DEVELOPMENT, INC.
DFT
R. RISON
6/12/75
CHK
ENG
PE
TITLE
DECODE SELECT
CARD 4 FIG 4-5
DWG NO
REV
SCALE
NEXT ASSY
SHT OF

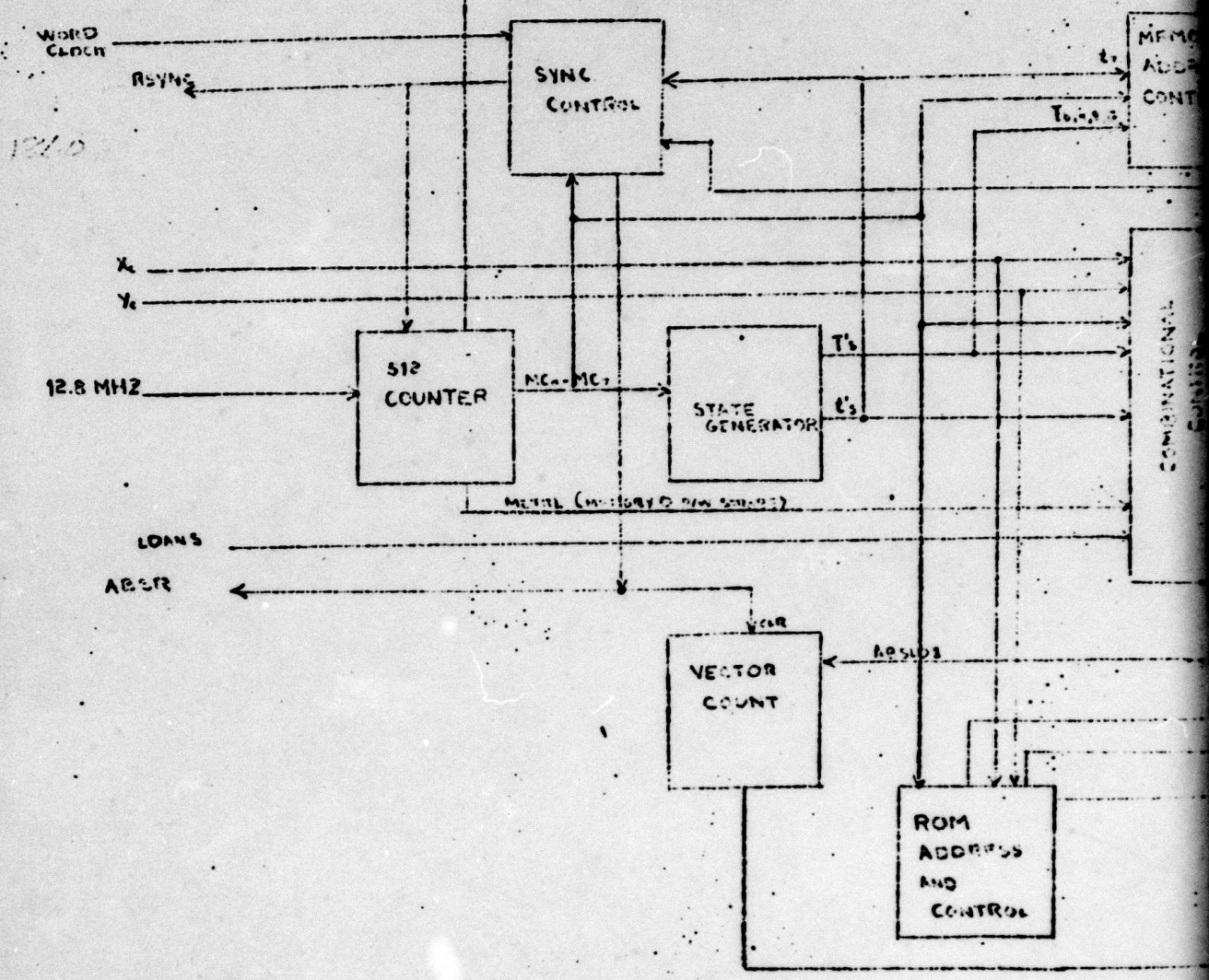


OUTPUT BIT REPRESENTATION									
FORMAT	XcYc	X_0	X_1	X_2	X_3	X_4	X_5	X_6	X_7
I	00	S*	VC_0	VC_1	VC_2	VC_3	VC_4	VC_5	SEL 1
II	01	S	VC_0	VC_1	VC_2	VC_3	VC_4	VC_5	SEL 1
III	10	S	VC_0	VC_1	VC_2	VC_3	VC_4	SEL 2	SEL 1
IV	11	S	VC_0	VC_1	VC_2	S	VC_0	VC_1	VC_2

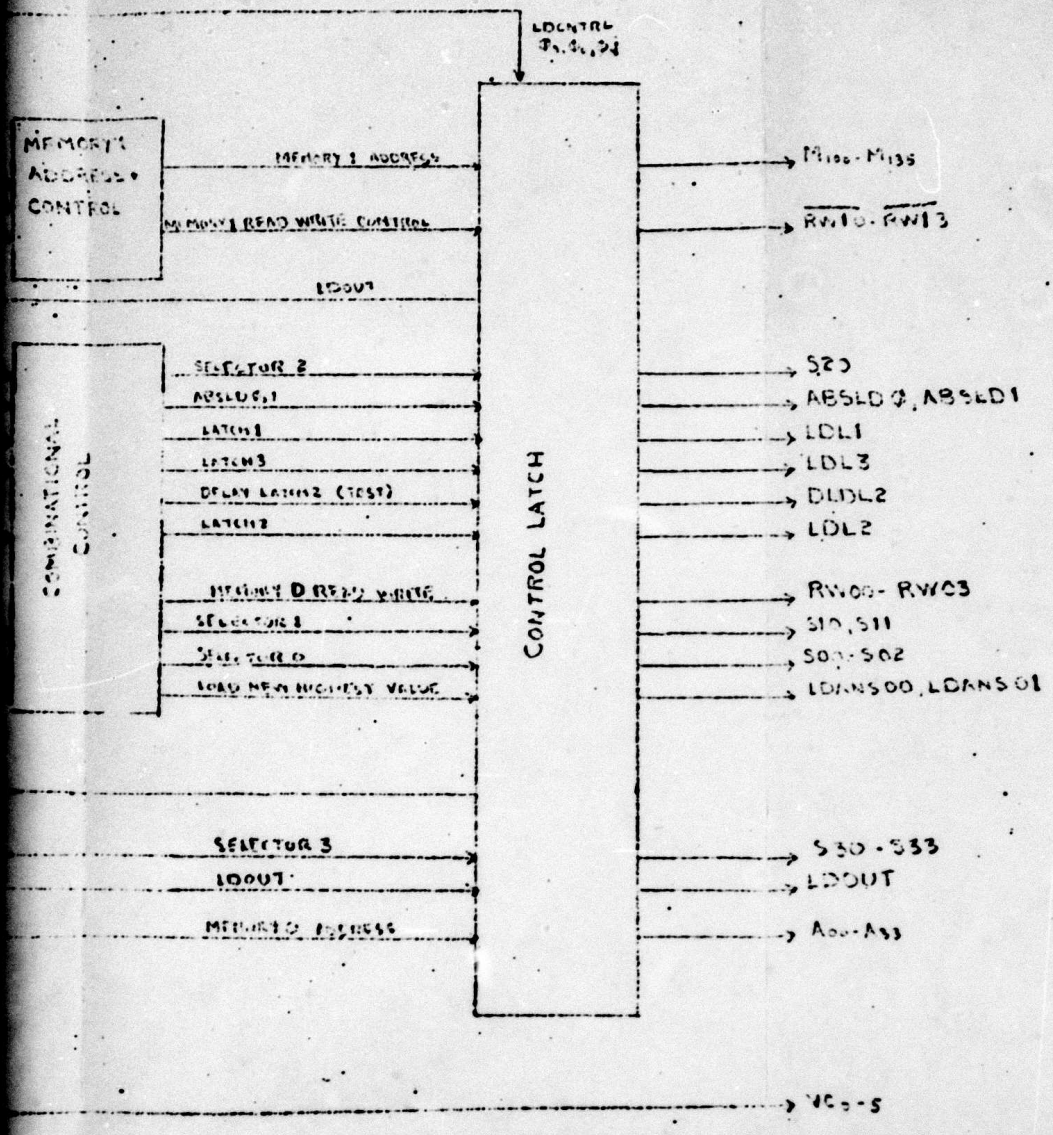
*S is sign of selected value

DATA/WARE DEVELOPMENT, INC.

DFT R. RISON	6/12/75	TITLE DECODER SELECT CARD 4 FIG 4-6
CHK		
ENG		DWG NO / REV
PE		SCALE / NEXT ASSY / SHT / OF

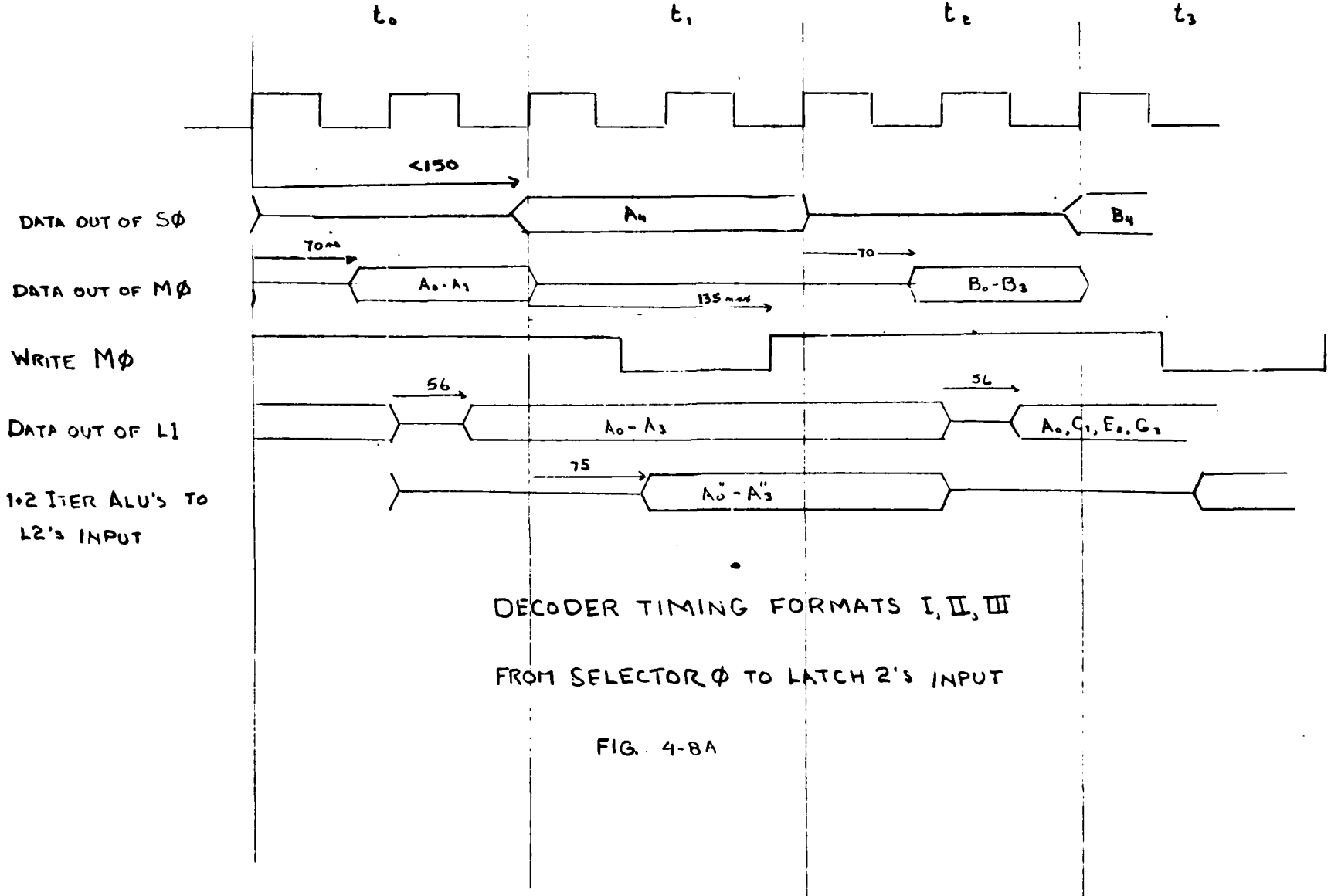


FIGURE



DATA/WARE DEVELOPMENT, INC.

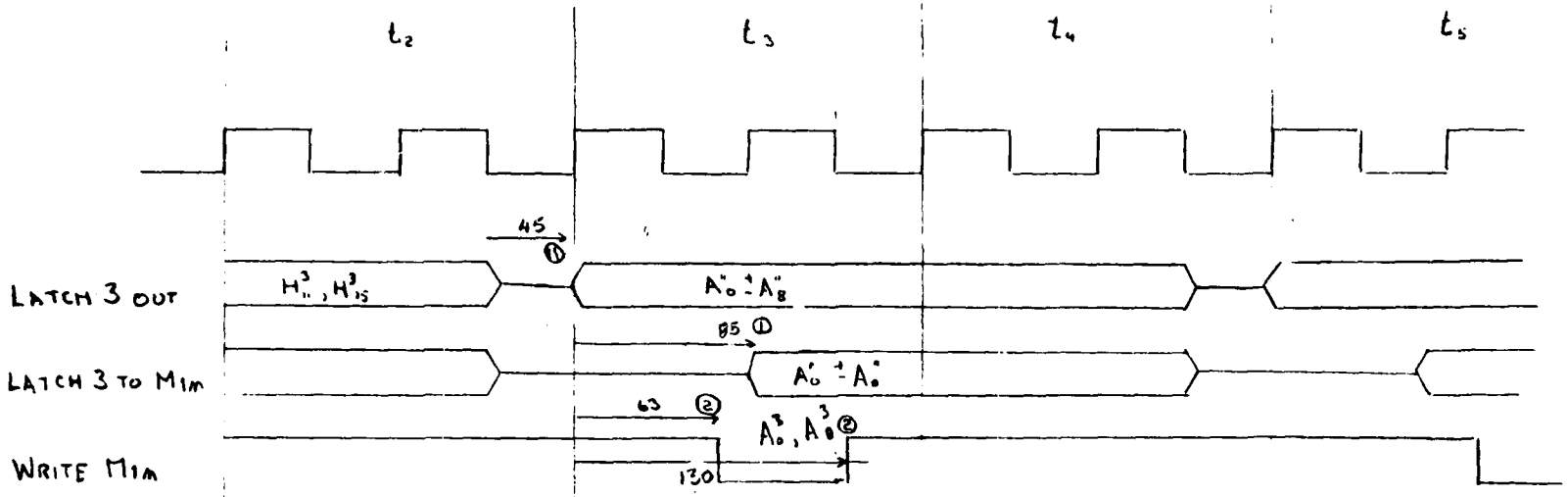
DFT		TITLE	CONTROL SECTION BLOCK DIAGRAM
CHK			
ENG		DWG NO	REV
PE		SCALE	NEXT ASSY / SHT



DECODER TIMING FORMATS I, II, III

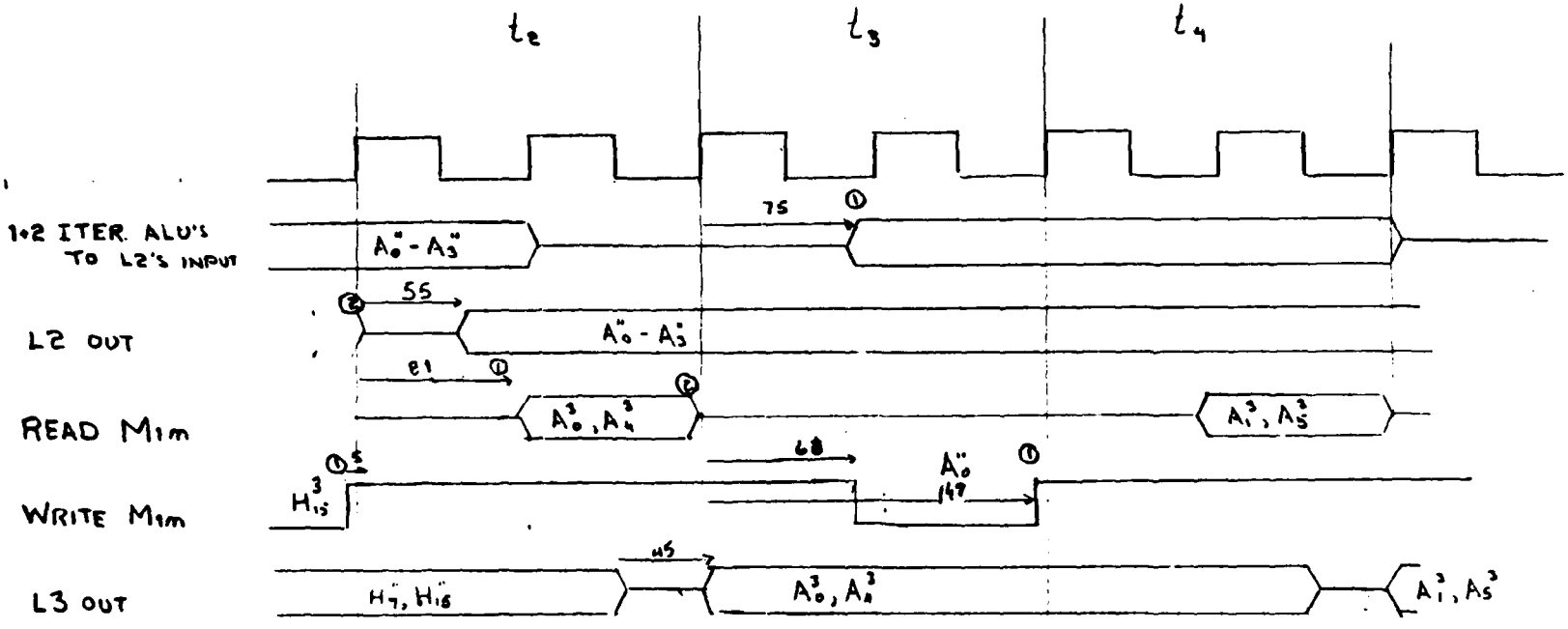
FROM SELECTOR Φ TO LATCH 2's INPUT

FIG. 4-8A



① SLOWEST TIME
② FASTEST TIME

FORMAT I T_{12}
FIG 4-8B

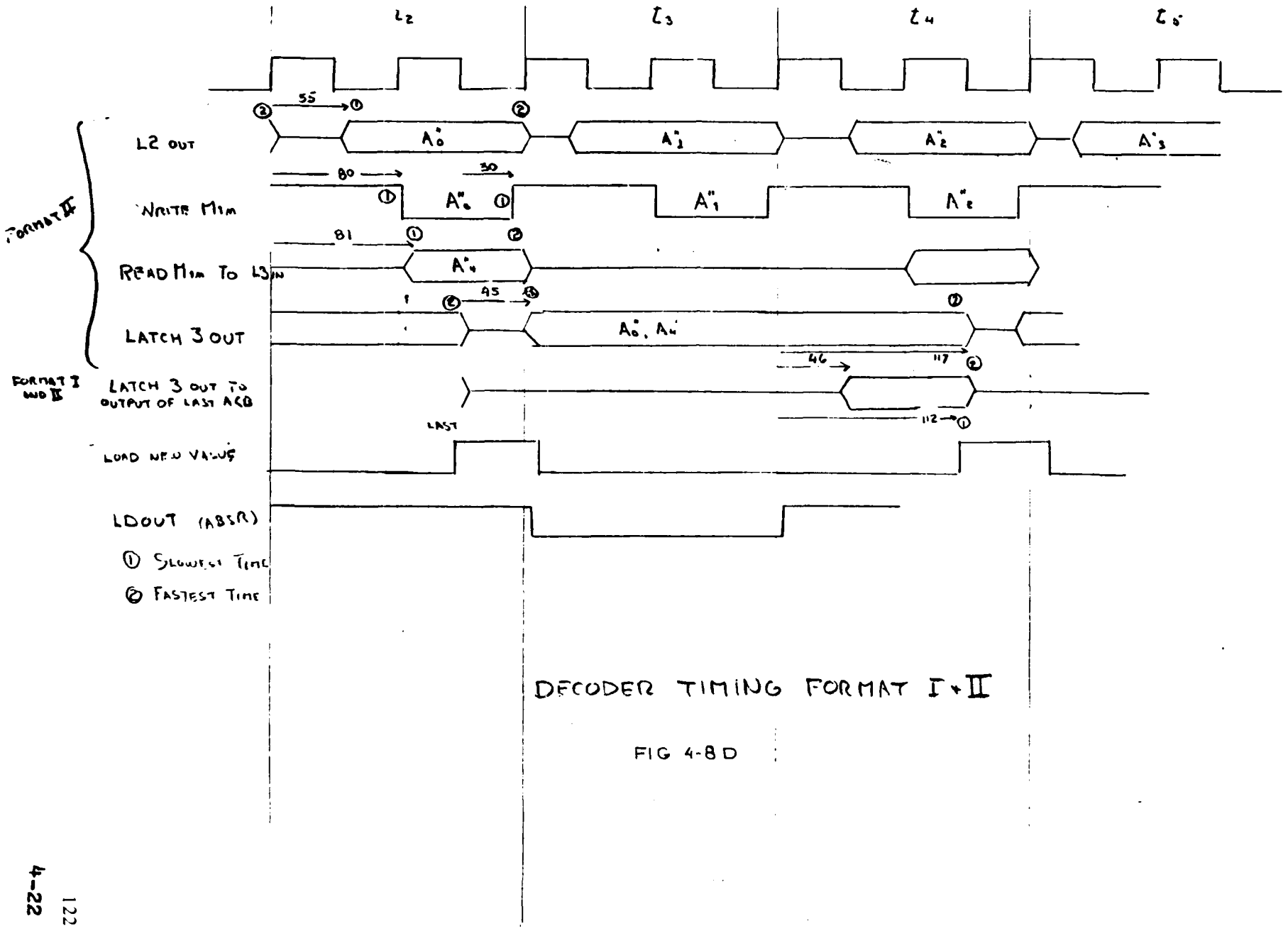


L3 TO FINAL COMPARE
SEE FORMAT II

FORMAT I T_4

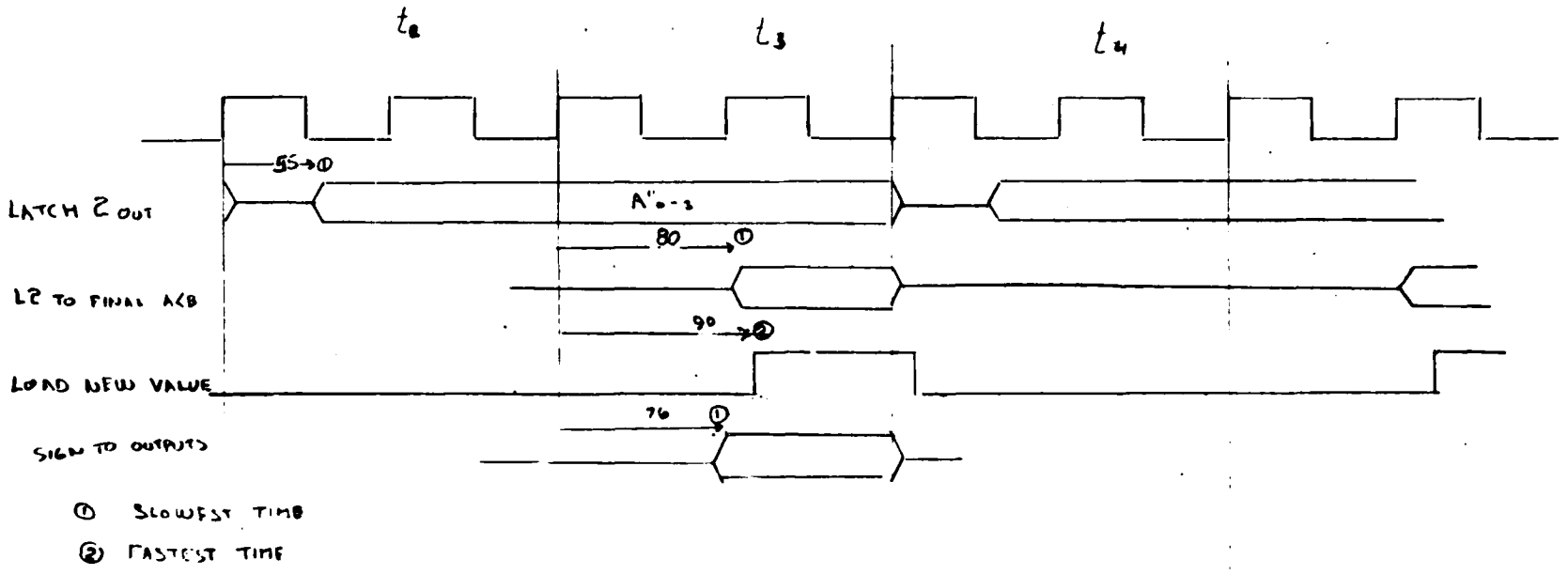
① SLOWEST TIME
② FASTEST TIME

FIG 4-8C



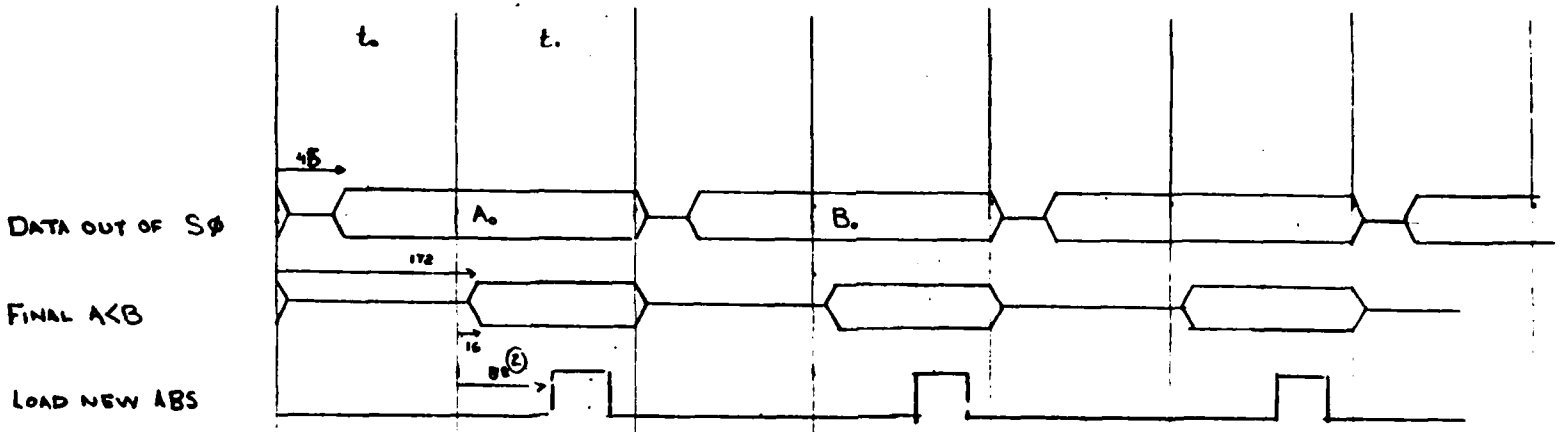
DECODER TIMING FORMAT I + II

FIG 4-8 D



DECODER TIMING FORMAT III

FIG 4-8E



DECODER FORMAT IV

FIG 4-8F

SYNCHRONIZATION PROCESSOR STUDY

A. Burke
The Magnavox Company

FWD75-1008

SYNCHRONIZATION PROCESSOR STUDY

23 May 1975

Contract N66001-75-C-0171

Prepared for the
Naval Undersea Center
San Diego, California

THE Magnavox COMPANY
GOVERNMENT AND INDUSTRIAL GROUP
FORT WAYNE DIVISION
Fort Wayne, Indiana

CONTENTS

ILLUSTRATIONS

ILLUSTRATIONS (CONT)

1.0 INTRODUCTION

The video link for the ARPA RPV must operate in a hostile electromagnetic environment wherein various forms of interference (both intentional and unintentional) can be expected to exist. Consequently much work has been performed in order to provide a margin of jam (AJ) protection for the video link. This work has revolved around transform encoding techniques which significantly reduce the bit rate of the video signal after transformation so that spread spectrum modulation techniques can be employed to provide the jam protection for the transmitted video signal. It was realized that the TV sync signal, (specifically the horizontal line scan synchronization pulse), should have a large margin of AJ protection, and that the generation, detection and processing of the sync information should be easy to implement (especially in the RPV); and acquisition should be rapid. In addition, it is considered desirable to utilize the vertical retrace blanking interval portion of each field for the transmission of sync information, leaving the horizontal retrace blanking interval at the end of each video line free for the transmission of ancillary data such as color information.

The use of a surface acoustic wave, phase shift key (PSK) matched filter for detection of the sync signal followed by a reentry delay line for predetection integration was postulated as a means for providing a theoretical 40 dB of processing gain for the synchronization signal. The results of studies intended to specify the design requirements of the components of such a system together with the expected performance of the system comprise the bulk of this report.

2.0 SCOPE OF STUDY

The synchronization system characteristics/requirements that were given at the outset of the study are as follows:

(1) Link transmission bandwidth - 20 MHz

(2) Sync signal time allotment - 1.27 millisec (20 horizontal scan lines from each field).

(3) Maximum possible time-bandwidth product for each sync signal - 44 dB.

(4) Acquisition time - Reliable horizontal sync pulses by the end of each sync sequence (within the first 20 lines of each field).

(5) Percentage of frame time horizontal sync signals provided to ground station video processor - 100%.

(6) Sync signal generation in RPV - Simple as possible and preferably all digital.

The specific areas studied and included in this report address the following topics:

(1) The video signal/sync signal format.

(2) The interface between the video signal generator and sync signal generator in the RPV flight vehicle.

(3) The interface between the ground station link receiver, video processor and sync processor.

(4) The design and characteristics of the sync processor matched filter.

(5) The design and characteristics of the sync processor pre-detection integrator (Recirculating Integrator).

(6) The design and characteristics of the sync detector algorithm and logic.

(7) Sync processor AGC characteristics.

(8) RF gain and dynamic range characteristics.

(9) The effect of oscillator stabilities on system performance.

(10) The effect of doppler on system performance.

3.0 SUMMARY

3.1 General

The objective of this study is to investigate a technique for providing protected horizontal line sync for the ARPA RPV TV sub-system. The proposed approach utilizes PN-PSK spread spectrum modulation in conjunction with surface acoustic wave (SAW) matched filtering and pre-detection integration to provide a high probability of rapid sync acquisition in the presence of interference. The vertical retrace blanking intervals of each field are used for transmission and processing of sync information leaving the remaining portion of the frames available for video information. Although sync information is transmitted for a small portion of a video frame, the system provides continuous horizontal sync information to the ground station video processor. The transmission bandwidth is 20 MHz, consistent with that proposed for the video data transmission.

3.2 RPV

The RPV Sync signal generator is inherently simple, can be implemented entirely with digital logic, and consumes 4 watts and about 22 cubic inches. The generator provides a stable clock to the RPV video processor which in turn provides synchronization information to the sync signal generator. The sync signal is generated by a feedback shift register which produces a 1250 chip PN sequence. This sequence is synchronized to the video sync pulses and has a repeat length equal to a horizontal scan line interval. Twenty of these sequences are utilized at the start of each video field. The digital output of the sync signal generator balance modulates a 138 MHz carrier and the resulting PSK signal is supplied to the down link transmitter.

3.3 Ground Station

The ground station portion of the sync processor is designed to interface with the TV link receiver at a 138 MHz IF frequency. This signal is applied to a noise limiter to avoid interference overload of subsequent processing stages. The noise limiter output is then applied to an array of six PN subsequence SAW matched filters, each processing one-sixth of the 1250 chip sequence, to yield a net theoretical processing gain of 31 dB for each of the 20 lines of sync information received. The matched filter outputs are combined on a SAW reentrant delay line which has a time delay equal to the horizontal scan. The reentrant delay line functions as a Recirculating Integrator (RI) to provide up to 12 dB of additional processing gain over the twenty line frame sync interval. The RI output is then envelope detected and applied to a tracking threshold detector (TTD) where a decision is made as to the presence or absence of received sync pulses. These decisions in which errors may be present, are converted to uniform 50 nsec pulses that are applied to the sync detector logic (SDL). The SDL analyzes the TTD output pulses and searches for those meeting the criteria for true sync pulses, i.e., a spacing equal to one horizontal scan time. When these pulses are found, the SDL tracks

them for several lines to verify their authenticity and then rapidly aligns the phase of a locally generated line rate pulse stream to that of the correct pulses while rejecting those due to noise. The resultant 50 nsec output pulses, which have a precise 15.75 KHz rate and are now in phase with those transmitted from the RPV, are then applied continuously to the ground station video processor. The phase thus determined remains fixed until a new sync signal is received.

3.4 SAW Device

Two types of SAW devices are used in the sync processor. The first is a set of six sub-sequence matched filters which are phase coded lines corresponding to the transmitted PN sequence. The six lines function as a single matched filter, which is segmented for fabrication purposes. The lines are designed for a 138 Mlz center frequency and have a nominal 20 Mlz bandwidth. The design of these devices is discussed in paragraph 5.3.2.3. The effects of frequency error and temperature variations on the filters is discussed in paragraph 6.0 where it is shown that these factors will not cause significant degradation in performance either for moderate temperature variations, or for reasonable frequency offsets due to oscillator drift and doppler.

The second type of SAW device used is a precision multiport delay line which is configured as a Recirculating Integrator. This device sums the output of the six matched filters and coherently accumulates these outputs during the twenty lines of sync signal inputs. The design requirements of the RI delay line with respect to temperature, delay error, and mechanical tolerances, and the theoretical performance of the Recirculating Integrator, is analyzed in paragraph 5.0. There it is concluded that these factors can be controlled to a degree adequate to realize a net 12 dB or more of processing gain from the RI in the absence of oscillator or doppler induced frequency offset.

The effects of frequency offset on the RI processing gain is analyzed in paragraph 6.0. There it is shown that frequency offset error due to frequency source inaccuracies and doppler shift would reduce the effective RI processing gain to negligible levels unless the frequency offset is corrected. Two methods for correcting the offset are briefly discussed.

3.5 Overall Sync Processor Performance

The performance of the sync processor is analyzed in the Sync Detector Logic subparagraphs of paragraph 5.0 and further in paragraph 6.2 where frequency offset effects are considered. The results of paragraph 5.3.3.3 show that with full RI processing gain the probability of achieving sync at SNR below -17.5 dB is better than .9999999 while the probability of obtaining false sync is negligible (less than one per million frames) over the entire frame interval.

The performance was also analyzed for the amounts of uncorrected frequency offsets that are anticipated due to doppler and frequency source error. For doppler alone, the frequency shifts at 4.5, 10, and 15 GHz and 100 knots RPV velocity are 772, 1715, and 2572 Hz respectively. The corresponding maximum RI processing gains for these offsets are shown to be 5.18, 1.99, and 0.68 dB. With offsets due to local oscillator frequency inaccuracies of 10^{-7} in the RPV and 10^{-8} at the ground station added to the doppler, the total frequency error becomes 1267 Hz at 4.5 GHz, 2815 Hz at 10 GHz, and 4222 Hz at 15 GHz. The maximum corresponding RI processing gains for these offsets are 3.15, 0.45, and 0.03 dB. If the frequency offset is not corrected the probability of acquiring sync is .995 at a -13 dB SNR although the probability of false sync remains low due to provisions in the Sync Detector Logic for avoiding false sync.

3.6 Results and Conclusions

Results from paragraph 5.3.3.3 show that the Sync Processor with a Recirculating Integrator can have a probability of acquiring sync approaching unity at a 10^{-1} video data error probability.

Further results from paragraph 6.2.2 indicate that frequency offset due to doppler and oscillator errors must be corrected in order to realize the processing gain potential of the RI. Therefore, it is recommended that the methods for correcting frequency offset be considered and pursued further.

4.0 DESCRIPTION OF CONCEPT

A functional diagram of the RPV/Ground Station video system is shown in Figure 1. In the RPV, input video information is processed so as to realize video bit rate reduction. The spectrum of the resultant video data stream is then spread spectrum modulated to a bandwidth of 20 MHz before transmission. In addition, a sync sequence consisting of a 1250 chip pseudorandom sequence clocked at a nominal 20 mbps rate, and phase shift key modulated onto a 138 MHz carrier is likewise supplied to the link transmitter. The format of the sync signal and video signal over one complete frame interval (1/30 sec) is illustrated in Figure 2. The video portion of each frame consists of two fields (video A and video B), which occupy lines 21 thru 262 and lines 284 thru 525 respectively. The sync signal is sent twice each frame (sync A and sync B), and it occupies lines 1 thru 20 and lines 264 thru 283 respectively.

The 1250 chip PN sequence is actually clocked at a 19.6875 MHz rate, thus the duration of each chip is 50.79 nanoseconds; and the total duration of the 1250 chip sequence is 63.492 μsecs, equal to one horizontal scan line time interval. The 1250 chip sequence is repeated 20 times during each of the two sync signal intervals per frame so that each sync signal occupies approximately 1.27 milliseconds. The total percentage sync signal occupancy per frame is 7.62%.

At the ground station, the sync signals are processed on a field by field basis. The maximum time-bandwidth product available per line is (63.492 μsec)(19.6875 MHz) = 1250, and the maximum time-bandwidth product per field is (20)(1250) = 2.5×10^4.

Each chip in the sync sequence contains 7 cycles of coherent 137.8125 MHz carrier resulting in a fractional bandwidth of 14.3%. The carrier choice represents a reasonable trade-off between such factors as insertion loss, surface wave device fabrication difficulty, and implementation of the sync signal generator in the RPV. The characteristics of the sync signal are summarized in Table 4-1.

The IF output of the ground station link receiver consists of the 137.8125 MHz PN-PSK modulated sync signal and the video information signal, and it is supplied to the sync processor and ground station video processor simultaneously. In the sync processor, the receiver IF output is correlated with a stored replica of the sync sequence in a 1250 chip surface wave device matched filter. Each time the matched filter receives the sync sequence, it produces a correlation pulse which consists of a burst of 137.8125 MHz carrier. In the ideal (non-bandlimited) case, the envelope of the correlation pulse exhibits the characteristic shape for a PN sequence. It is triangular in shape and its width at the half amplitude point equals the reciprocal of the chip rate (50.8 nanosecs in this case). (See Figure 3a.) The peak of the correlation pulse represents the maximum signal to noise ratio at the output of the matched filter; and

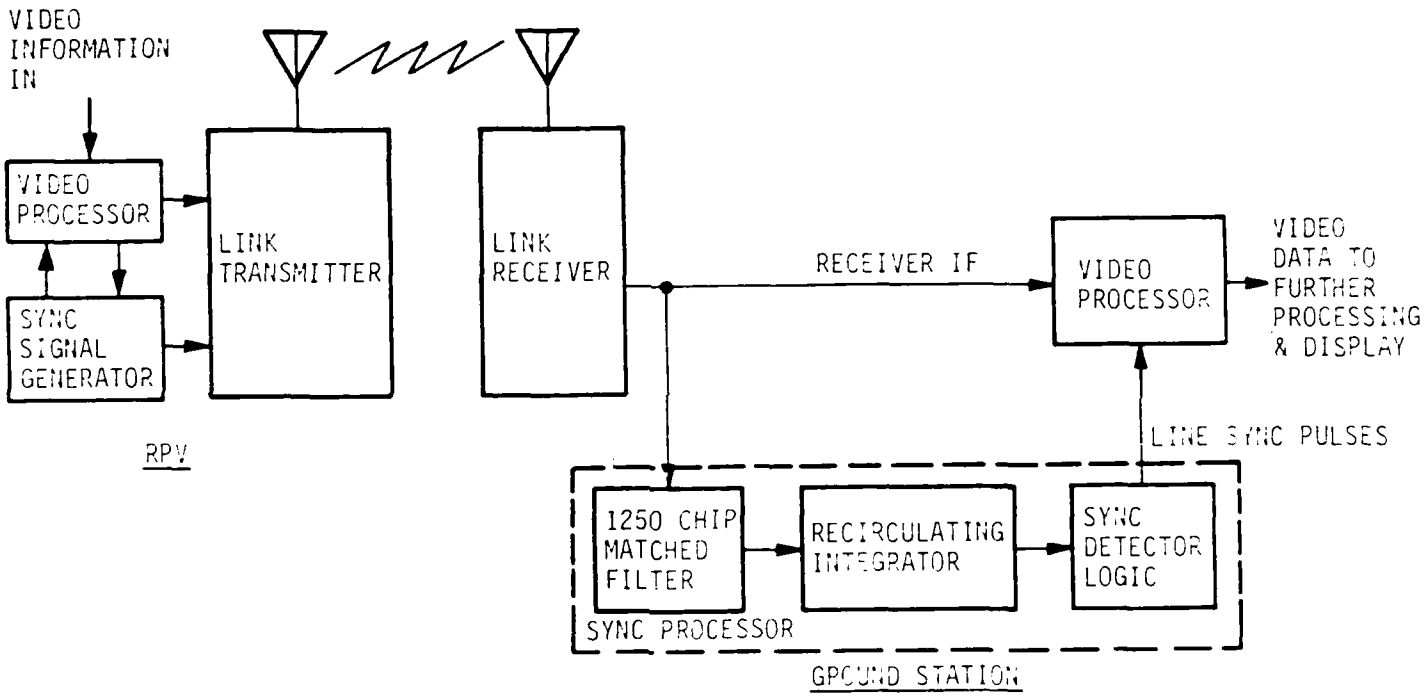
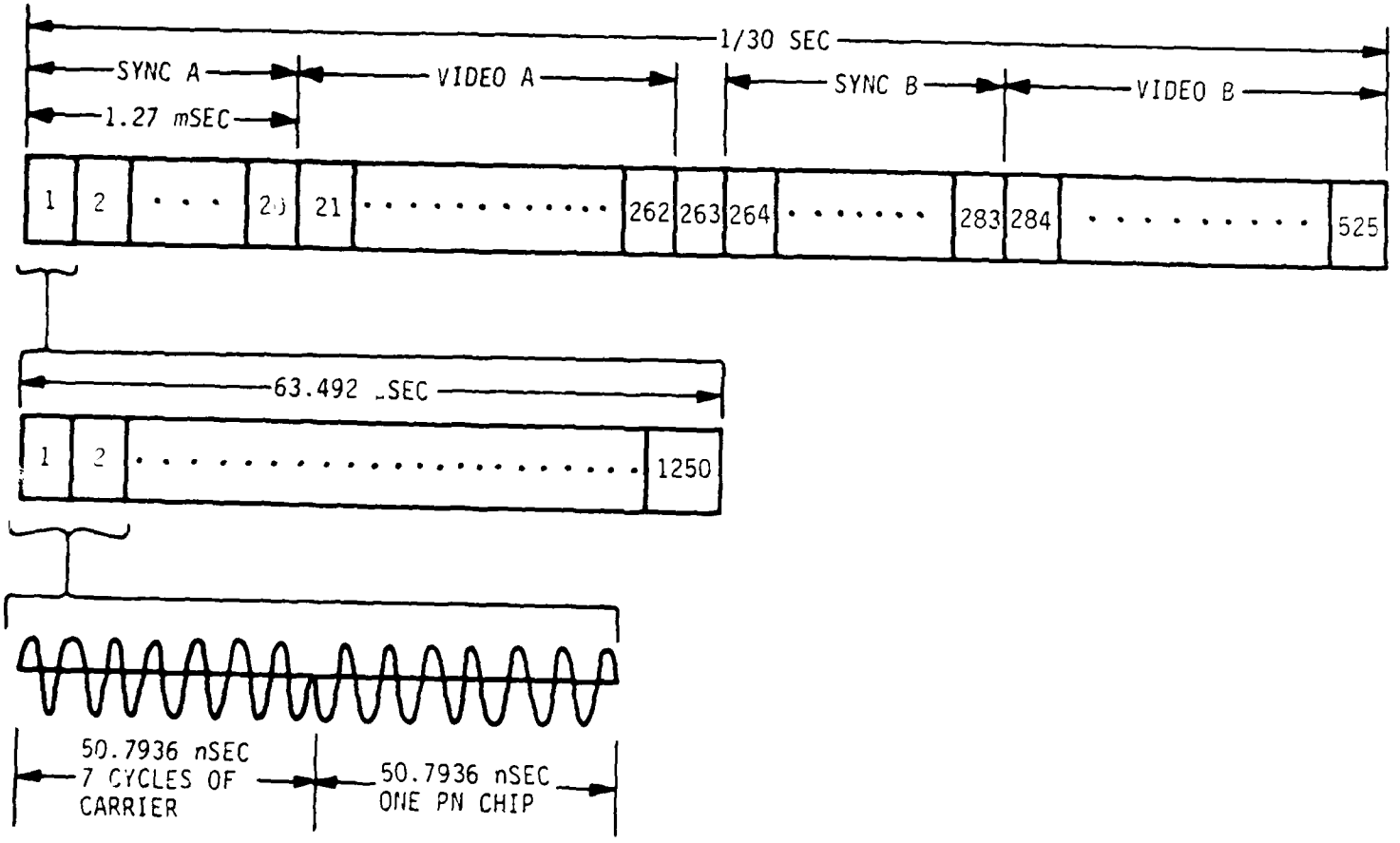
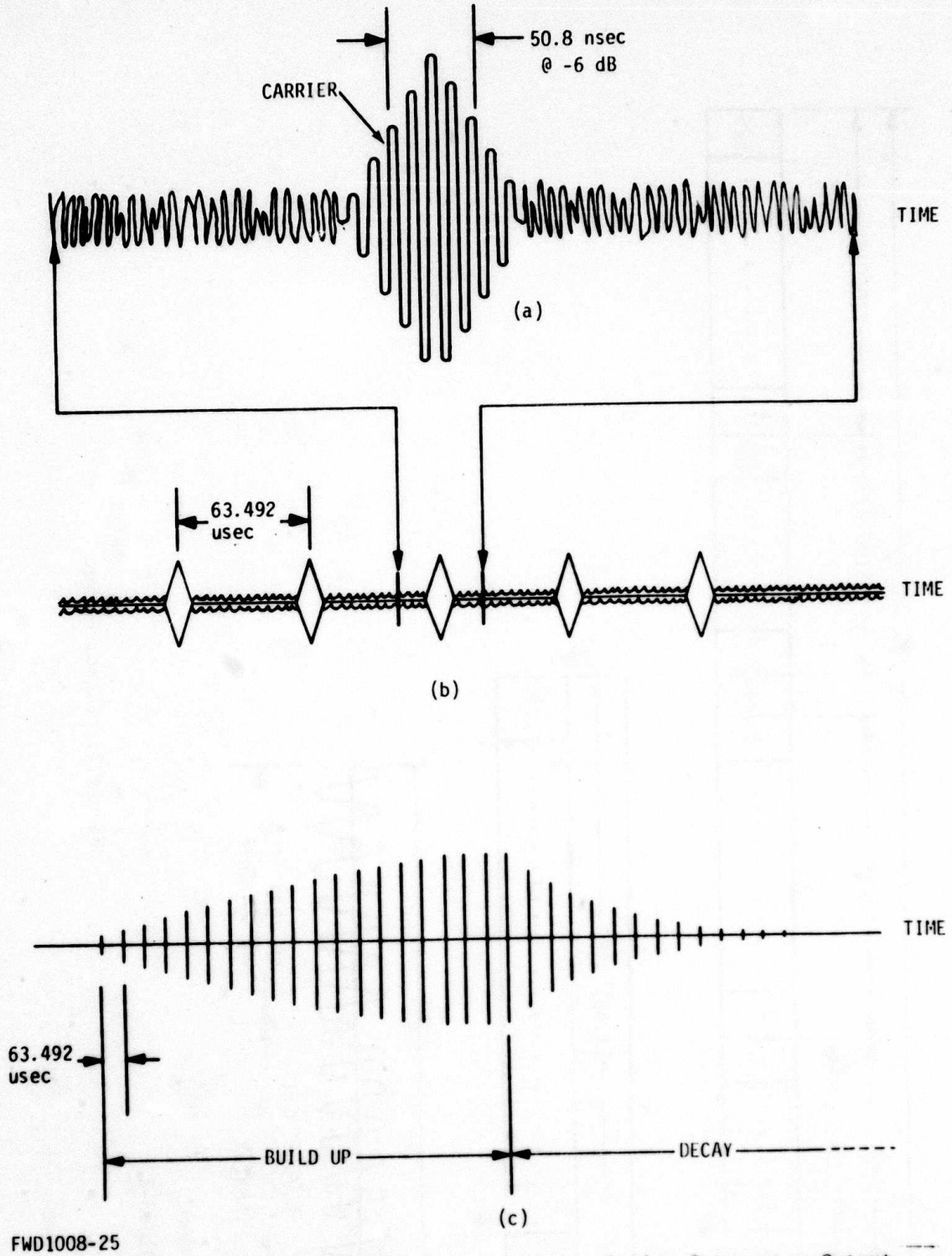


Figure 1. Basic System



FWD1008-2

Figure 2. Signal Format



FWD1008-25

Figure 3. Matched Filter Output, Recirculating Integrator Output

Table 4-1. Summary of Sync Signal Characteristics

Sync Sequence	1250 Chip pseudo random code
Sync sequence duration	63.492 μsec
Sync sequence chip rate	19.6875 MHz
# sequences/sync signal	20
Sync signal duration	1.27 msec
Sync signal repetition rate	Once per field
Sync signal occupancy per frame	7.62%
Sync signal carrier frequency	137.8125 MHz
Sync signal fractional bandwidth	14.3%
Time-bandwidth product per sequence	1250
Time-bandwidth product per field	2.5×10^4

if the output of the matched filter is sampled at the peak, a signal to noise ratio improvement equal to the time-bandwidth product of the input signal[1] would be realized (31 dB for a 1250 chip sequence).

The matched filter receives a series of 20 sync sequences during each sync signal interval, and it produces a series of 20 correlation pulses separated in time by the sequence period length (63.492 usec) as shown in Figure 3b. The intervals between correlation pulses consist of receiver input noise suppressed by the processing gain of the matched filter, and the autocorrelation side lobes associated with the 1250 chip PN sequence.

The output of the matched filter[2] is fed to a Recirculating Integrater, (RI), which consists of a surface wave re-entry delay line and a feed back loop, both operating at the IF frequency. The output of the delay line is returned to its input through the feedback loop. The delay line-feedback loop time delay is precisely 63.492 μsecs so that successive correlation pulse outputs from the matched filter add. (The carrier segments under the correlation pulse envelopes add in phase.) If the net RI loop gain is less than unity, the output of the RI grows exponentially as shown in Figure 3c. The addition of successive correlation pulses in the RI amounts to predetection integration of the sync sequence over the sync

---

[1] In Gaussian noise with no band limiting.

[2] In practice, the matched filter is broken into six sub-sections whose outputs are combined on the Recirculating Integrator Delay Line. This technique is discussed in the sections to follow.

signal interval and yields an increase in processing gain over that obtained from a single sync sequence. (The processing gain characteristics of the RI are discussed in a later section.) When the 20 sync sequences comprising a sync interval are completed, the matched filter no longer produces correlation pulses and the output of the RI decays exponentially towards zero as shown in Figure 3c.

The output of the Recirculating Integrator is fed to a sync detector which envelope detects the correlation pulses from the RI and compares the time of occurence of the RI output pulses with 1250 quantized phases of a stable 19.6875 MHz clock. After a suitable number of RI output pulses have been detected, one of the 1250 phases of the 19.6875 MHz clock is selected that corresponds to the time position of the RI output pulses. This selected phase then repeats every 63.492 μsec in time synchronism with the RI output pulses.

The line sync pulses generated by the sync detector logic are then applied to the ground station video processor (Figure 1). Thus, once the phase of the 15.750 KHz pulses is correctly oriented, the time position of the line sync pulses fed to the video processor bears a fixed time relationship to the end of each 1250 chip sync sequence transmitted. Since the 19.6875 MHz clock is stable over the field period, the line sync pulses supplied to the video processor are correctly timed over the entire field even though the sync signal is only present during 20 lines of the field.

The technique of selecting a particular phase of a stable clock to coincide with the horizontal sync pulses eliminates the need for a phase lock loop to track correlation peaks. This results in rapid acquisition and is useful for single frame or "snap shot" transmissions from the RPV.

5.0 SYSTEM DESIGN

The analysis of the characteristics and design requirements on the various components of the sync processor system were based on a system that could, in theory, provide most of the processing gain inherent in the time-bandwidth product available for the sync signal. With the exception of the surface wave devices, the system was considered in terms of off-the-shelf hardware that could readily be obtained and employed in a breadboard model of the system.

5.1 RPV Electronics

The sync signal generation portion of the RPV electronics consists of a temperature compensated crystal oscillator, a 1250 chip sync sequence generator, a balanced modulator, and some additional logic used to control the generation of the sync sequence and to interface with the RPV video electronics and down link transmitter (see Figure 4).

The oscillator provides a 137.8125 MHz output which drives a buffer amplifier and a high speed (ECL) divide-by-seven counter. The output of the buffer amplifier is used to supply the balanced modulator with 137.8125 MHz carrier at a nominal power level of +7 dBm. The output of the divide-by-seven counter is a coherent 19.6875 MHz clock which is used to drive the 1250 chip sync sequence generator, and which is also provided as a clock output to drive the RPV video processor electronics.

The 1250 chip sync sequence generator has two outputs. The main output is the baseband 1250 chip sync sequence which is supplied to the modulation input of the balanced modulator. The second output is the "initializing" state of the 1250 chip sync sequence generator which occurs at the beginning of each 1250 chip sequence. This output repeats at a 15.750 kHz rate and is used by the line counter which keeps track of the line count number within a frame.

At the beginning of each frame, a frame position ID pulse is received from the RPV video electronics which sets the line counter to a count of zero and synchronizes the sync signal generator to the RPV video electronics. The line counter then counts 15.750 kHz pulses from the sync sequence generator, and in doing so, keeps track of the line number within the frame. After it has counted 525 lines, it is reset to zero again by the frame position ID pulse and the process repeats.

The output states of the line rate counter, (a ten stage counter is adequate for this purpose), are fed to a set of recognition gates which decode the output of the line counter to form a "sync active/passive" logic level which is supplied to the down link transmitter. The sync active/passive signal is used by the transmitter to select its signal source (i.e., sync signal from the balanced modulator, or video signal from the RPV video electronics). The "sync active" condition is indicated to the transmitter when the line counter contains a count of

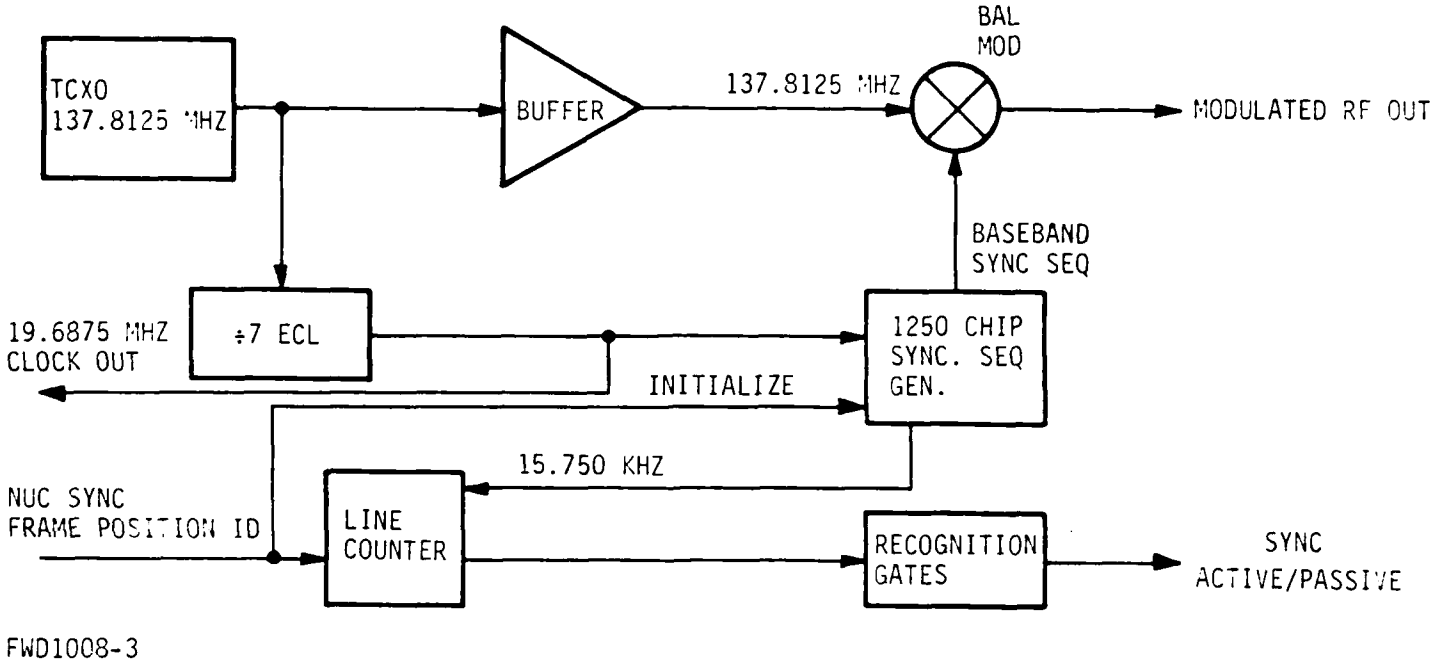


Figure 4. RPV A/C Terminal

0 thru 19 or 263 thru 282, which corresponds to frame lines 1 thru 20 and 264 thru 283. In this situation the link transmitter selects the output of the balanced modulator as its signal source. The "sync passive" condition is indicated to the transmitter when the line counter contains a count of 20 thru 261 or 283 thru 524, which corresponds to frame lines 21 thru 262 and 284 thru 525. In this situation the transmitter selects the RPV video electronics as its signal source (see Figure 2).

The 1250 chip sync sequence is implemented by using an eleven stage feedback shift register augmented by an eleven bit decoder. The feedback shift register forms a 2047 chip maximal linear sequence which is truncated at the 1250th chip. The shift register is initialized to a predetermined state by the frame position ID pulse mentioned previously (see Figure 4) so that the 1250 chip sync sequence is properly synchronized relative to the start of the frame. After 1250 clock pulses from the 19.6875 MHz clock, the feedback shift register is in its "1250" state (equivalent to the end of the first line of sync) and the corresponding eleven bits in the shift register are recognized by the eleven bit decoder. The decoder then reinitializes the shift register to its initial state so that the sync sequence may be repeated.

The balanced modulator can be implemented using standard techniques, i.e., a double balanced mixer can be used. This normally requires that a bipolar power supply is available in order to provide a symmetrical bipolar drive at the modulation port of the mixer. As an alternate approach, a high speed ECL Exclusive-OR could be employed as the modulator if followed by a suitable filter. The 137.8125 MHz carrier would comprise one input to the Exclusive-OR, and the 19.6875 MHz PN modulation from the 1250 chip sync sequence generator would comprise the other input. The output of the device would be a 137.8125 MHz square wave, bi-phase modulated by the sync sequence. A simple filter could then be used to select the 137.8125 MHz fundamental and the modulation sidebands. The use of the Exclusive-OR modulator seems an attractive alternate to the use of an analog modulator as it would allow the sync generation equipment to be all digital except for the oscillator and filter.

5.2 Physical Characteristics of RPV Electronics

The RPV electronics described above can be implemented with approximately eighteen standard ECL integrated circuits and a Temperature Compensated Crystal Oscillator (TCXO). The components could be installed on a standard printed circuit board with an area of eighteen square inches. The logic power requirement is five volts at two watts maximum. The TCXO is configured in a 2 x 2 x 4 inch package and consumes two watts of power at 28 Vdc. The total package would be approximately twenty-two cubic inches and would require four watts power.

5.3 Sync Processor

5.3.1 Analog Signal Flow Analysis

In determining the layout of the sync processor RF electronics it was assumed that the link receiver IF output power level would be main-

tained essentially constant by the receiver AGC once the input signal to noise ratio got above 0 dB. This assumption simplifies the dynamic range requirements of the sync processor RF electronics and allows the surface wave devices to be operated at signal power levels that minimize system noise floor problems. Specific RPV link transmission frequencies were not known, but it was postulated that they might be in the 4.5-5 GHz or the 10-15 GHz region based upon spectrum allocations presently being considered for RPV. A receiver noise figure of 10 dB was assumed as this should be readily obtainable at these frequencies.

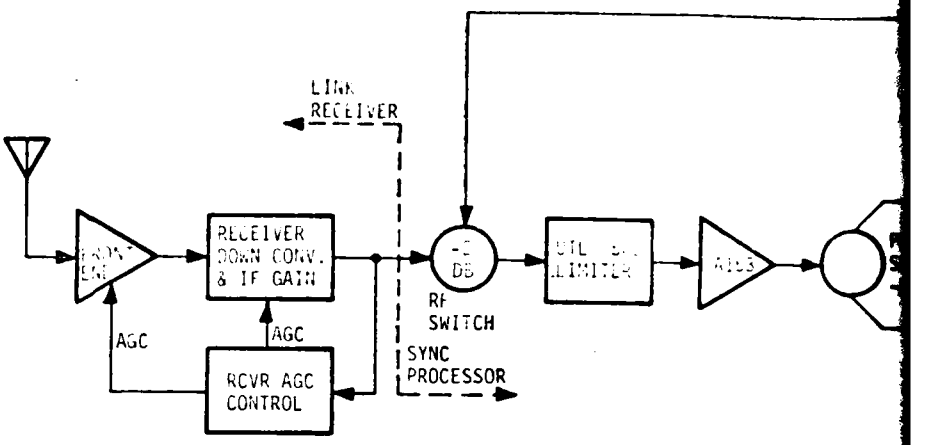
A block diagram of the sync processor indicating the various subsystem components is shown in Figure 5 together with the signal and noise power level distribution at various points in the system. A link receiver is included in the diagram to illustrate the interplay between the receiver and sync processor. The equivalent (thermal) noise level at the receiver input is -91 dBm based on a 20 MHz bandwidth and 10 dB receiver noise figure. The case is shown for a -15 dB signal to (thermal) noise power ratio at the receiver input, i.e., equivalent sync signal level at -106 dBm.

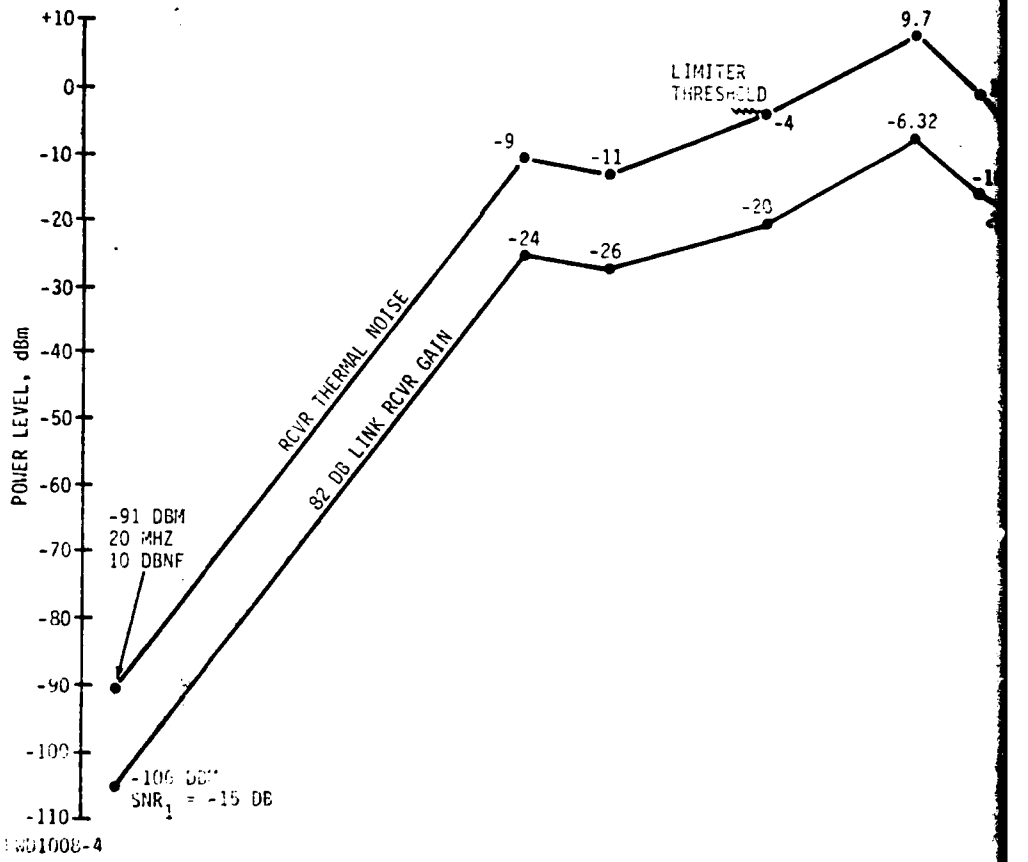
At the receiver IF output the signal and noise power levels are -24 dBm and -9 dBm respectively and form a composite signal whose power level is approximately -9 dBm. The composite signal is fed thru an RF switch (which forms part of the sync processor automatic level control (ALC), to be described later) and it is supplied to a band-pass limiter which maintains a constant power output of -4 dBm for limiter input signals (or noise) greater than -11 dBm. In this example, the limiter is in saturation on the noise component of the composite signal, and consequently the limiter output signal to noise ratio is degraded approximately 1 dB* by the action of the limiter. If pulse jamming occurs which the receiver AGC cannot follow, and if it exceeds the input signal level by more than approximately 15 dB, the jamming pulses are clipped by the action of the limiter so that large pulses of energy are not fed to the downstream RF gain and signal processing.

The link receiver AGC is inoperative until the received signal power level reaches approximately -91 dBm at which point the composite signal power at the receiver input is -88 dBm, and the composite signal power into the limiter is -8 dBm. For receiver input signal levels greater than -91 dBm, the receiver AGC activates and maintains a constant limiter input signal level of -8 dBm. Consequently, the action of the receiver AGC and limiter maintain the variation in signal component level supplied to the matched filter to about 16 dB because, as the received signal to noise ratio increases above -15 dB, a larger proportion of the limiter output power is allocated to signal and less is allocated to noise since the total limiter output power is constant.

- -

* Gardner, "Phaselock Techniques", John Wiley and Sons, Inc., pp. 55-57.


LINK
RECEIVER
RECEIVER
DOWN CONV.
& IF GAIN
AGC
AGC
RCVR AGC
CONTROL
RF
SWITCH
SYNC
PROCESSOR


+10
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-110
POWER LEVEL, dBm
LIMITER
THRESHOLD
9.7
-4
-9
-11
-6.32
-20
-24
-26
RCVR THERMAL NOISE
82 DB LINK RCVR GAIN
-91 DBM
20 MHZ
10 DBNF
-106 DBM
SNR1 = -15 DB
WD1008-4

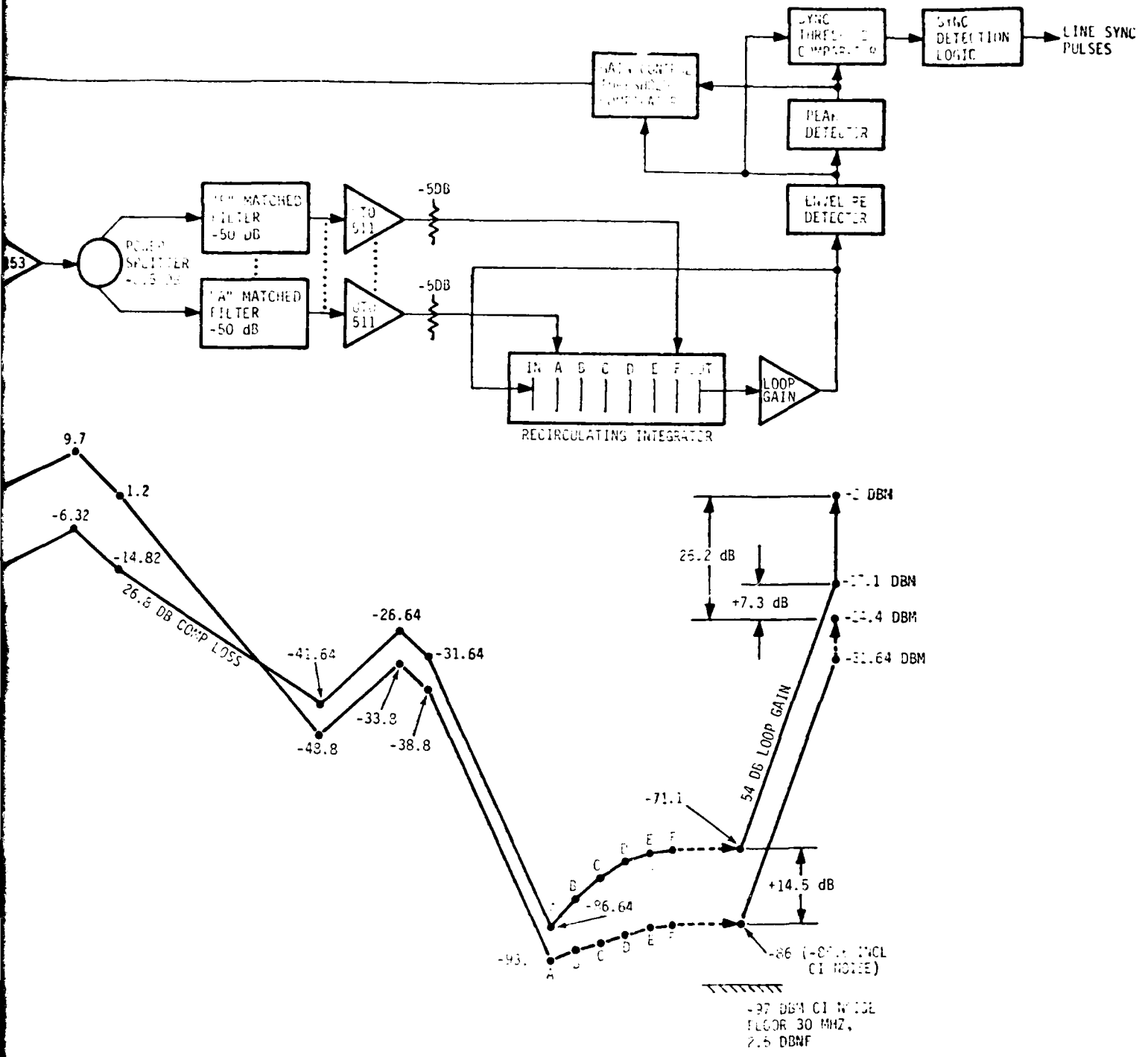


Figure 5 Ground Station Signal Flow Diagram

The composite limiter output is amplified and then split into six identical components by a reactive hybrid. These six components are then applied to six surface wave device sub-sequence matched filters labeled "A" thru "F" in Figure 5. Each sub-sequence matched filter (SSMF) encompasses a different segment (1/6) of the sync sequence code. (It is impractical to built a single surface wave device matched filter 63.492 μs long*.)

Since the sub-sequence matched filters are driven in parallel, the response of each SSMF to its corresponding portion of the incoming sync sequence is a sub-sequence correlation pulse, delayed by approximately 10.58 μs relative to the response of the previous SSMF. Each sub-sequence correlation response must be properly added in time to obtain the desired auto-correlation response of the sync sequence code. Addition of the sub-sequence correlations is performed on the Recirculating Integrator delay line to be discussed shortly.

Referring to Figure 5, the signal input power for each sub-sequence matched filter is -14.8 dBm, and the noise power is +1.2 dBm, based upon the receiver input signal to noise ratio assumed for this case. The insertion loss of each sub-sequence matched filter will be about 50 dB, and the noise power at the output of each will be about -48.8 dBm. But since the sub-sequence matched filters are matched to their corresponding segments of the sync sequence, each sub-sequence correlation will exhibit a compression gain of $10 \log_{10} (\frac{1250}{6}) = 23.2$ dB, so that the net compression gain of each sub-sequence matched filter will be about -26.8 dB. Thus, for a -14.8 dBm signal into the sub-sequence matched filters, the peak value of each sub-sequence correlation will be about -41.6 dBm.

The output of each sub-sequence matched filter is amplified (about 15 dB) by an integral amplifier contained in each sub-sequence matched filter module. The amplifiers provide buffering between the output matching networks on the sub-sequence matched filters and the corresponding input matching networks on the Recirculating Integrator delay line, in addition, they provide a drive level to the RI sufficient to reduce noise floor degradation of the signal to a minimum amount. Nominal 5 dB pads are included between each sub-sequence output amplifier and RI input to allow for variations in net insertion loss between the power splitter outputs and RI inputs for the six sub-sequence channels.

The Recirculating Integrator consists of the Recirculating Integrator Delay Line and feedback loop, as mentioned previously. The RI performs two functions; it adds the output of the sub-sequence matched filters in the proper time order to obtain the auto-correlation function of the sync sequence every time it is received, and it provides a precise 63.492 μs time delay to allow coherent summation of the 20 sync sequence auto-correlation pulses that occur in each sync signal interval.

- -

*The design of the sub-sequence matched filters is covered in the surface wave device section to follow.

As shown in Figure 5, the RI has a total of 8 transducers, which are labeled "A" thru "F", "OUT", and "IN", the A thru F transducers being driven by the sub-sequence matched filter outputs. The sub-sequence correlations occur in time order; i.e., sub-sequence correlation B lags sub-sequence correlation A by 10.58 μs, sub-sequence C lags that of B by 10.58 μs, etc. The A thru F transducers are separated by a distance corresponding to the time delay between sub-sequence correlations. When sub-sequence correlation A occurs, the A transducer of the RI generates a surface wave component which propagates towards the B transducer, arriving at the precise instant the B transducer is being excited by the B sub-sequence correlation. These wave components add linearly and propagate toward the C transducer. As the resultant surface wave propagates down the delay line, passing beneath successive transducers, each transducer adds to the signal such that, after passing the F transducer, the resultant surface wave represents the properly added contributions from the six sub-sequence matched filters. The resultant signal at the output transducer is the auto-correlation function of the 1250 chip sync sequence.

The insertion loss of the RI can be expected to be 55 dB* or less (55 dB was assumed for this analysis). Therefore, the signal and noise output components of the sub-sequence matched filters can be thought of as suffering 55 dB loss as measured at the RI output transducer. This is depicted graphically in the power level diagram of Figure 5, point "A", by indicating a peak sub-sequence "A" signal component at -86.6 dBm, and a noise component at -93.8 dBm for corresponding inputs at the "A" RI input transducer of -31.6 dBm and -38.8 dBm respectively. As sub-sequence correlation contributions are made to the signal at transducers B thru F, the equivalent peak correlation pulse amplitude that appears at the output transducer "grows" to a value of -71.1 dBm since the sub-sequence correlation contributions add linearly. On the other hand, the noise contributions at points A thru F add quadratically, assuming statistically independent noise sample contributions. Therefore, the noise power at the RI output grows to -86 dBm. Thus, for one 1250 chip sync sequence received at a -15 dB signal to noise ratio at the receiver input, the corresponding peak signal to noise ratio appearing at the RI output is +14.9 dB. Note that this to be expected since a 1250 chip PN sequence should provide 30.9 dB of processing gain. Therefore, for a -15 dB received signal to noise ratio and 1 dB limiter signal to noise loss, the peak signal to noise ratio at the output of the matched filter should be 30.9 dB - 15 dB - 1 dB = + 14.9 dB.

Actually, an accounting of the total noise power at the RI output must include the noise power contributed by the RI output amplifier. A cascade of wide-band amplifiers is necessary to provide the total loop gain needed for operation of the Recirculating Integrator. The noise figure, and hence the equivalent noise power contribution from the RI output amplifier will essentially be controlled by the first amplifier in

---

*See Surface Wave Device section.

the cascade. The output amplifier can be made using off the shelf MIC amplifiers designed for wide-band cascade operation, and it is possible to obtain a 2.5 dB noise figure from such amplifiers at the operating frequency of the RI.

Considering a 30 MHz RI operating bandwidth [a 30 MHz bandwidth is employed to avoid band limiting effects in the operation of the Recirculating Integrator], the equivalent noise power or noise floor, at the loop gain amplifier input is -97 dBm. When this noise contribution is added to the processed receiver noise, the net equivalent noise power at the Recirculating Integrator output is increased by 0.4 dB to -85.6 dBm. Therefore, the noise floor of the Recirculating Integrator delay line, considered as the matched filter output, has a negligible effect of processing gain.

The characteristics of the Recirculating Integrator when processing the aperiodically occuring sync sequence can be understood by considering the action of the feedback from RI output to input. When a sync sequence correlation pulse occurs at the output of the RI, it is amplified and then fed back to the RI input transducer. If the time delay between the input and output transducers is exactly 63.492 μs, a correlation pulse that is fed back from the output to the input of the RI will appear back at the output transducer at the precise instant that the next correlation pulse resulting from the sync signal arrives at the output transducer, since the correlation pulses occur once every 63.492 μs. The result is an addition of the new and fed back correlation pulse. The result of this addition is fed back to the RI input and is added to the next correlation pulse.

If the product of the RI insertion loss and the feedback loop gain is defined as a net loop gain α, the signal buildup characteristics of the Recirculating Integrator can be calculated as follows. Each correlation pulse can be considered as a signal voltage pulse s(t). If N such pulses are added on the Recirculating Integrator, the output of the Recirculating Integrator can be written as

$$s_o = s(t) + \alpha\, s(t) + \alpha^2 s(t) + \ldots + \alpha^{N-1} s(t)$$

$$= s(t) \sum_{K=0}^{N-1} \alpha^K = s(t)\, \frac{(1-\alpha^N)}{(1-\alpha)} \qquad (1)$$

The noise associated with the correlation pulses can be considered to be statistically independent noise voltage samples n_i each of rms value $\bar{n}$. Since the noise voltage samples are independent, the noise output of the Recirculating Integrator, n_o, for L noise samples is the RMS value of the noise samples weighted by the net loop gain α; that is,

$$\bar{n}_o = \sqrt{(\bar{n}_0)^2 + (\alpha\,\bar{n}_1)^2 + (\alpha^2\,\bar{n}_2)^2 + \ldots\ (\alpha^{L-1}\bar{n}_{L-1})^2}$$

$$= \sqrt{(\bar{n})^2\,[1 + \alpha^2 + \alpha^4 + \ldots\ \alpha^{2(L-1)}]}$$

$$= \bar{n}\sqrt{\sum_{K=0}^{L-1} \alpha^{2K}} = \bar{n}\sqrt{\frac{(1-\alpha^{2L})}{(1-\alpha^2)}} \qquad (2)$$

Since the noise signal is always present whether or not the sync signal is present, the noise output of the Recirculating Integrator must be considered as the result of an infinite number of noise samples, i.e.,

$$\bar{n}_o = \lim_{L\to\infty} \bar{n}\sqrt{\frac{(1-\alpha^{2L})}{(1-\alpha^2)}} = \frac{\bar{n}}{\sqrt{1-\alpha^2}} \quad \text{for } \alpha < 1^*. \qquad (3)$$

The signal to noise ratio at the output of the Recirculating Integrator after the addition of N correlation pulses is, therefore,

$$(SNR)_0 = \frac{s_o^2}{n_0^2} = \frac{s^2(t)}{\bar{n}^2}\ \frac{(1-\alpha^N)^2\ (1-\alpha^2)}{(1-\alpha)^2}$$

$$= \frac{(1-\alpha^N)^2\ (1+\alpha)}{(1-\alpha)}\ \frac{s^2(t)}{\bar{n}^2}\ . \qquad (4)$$

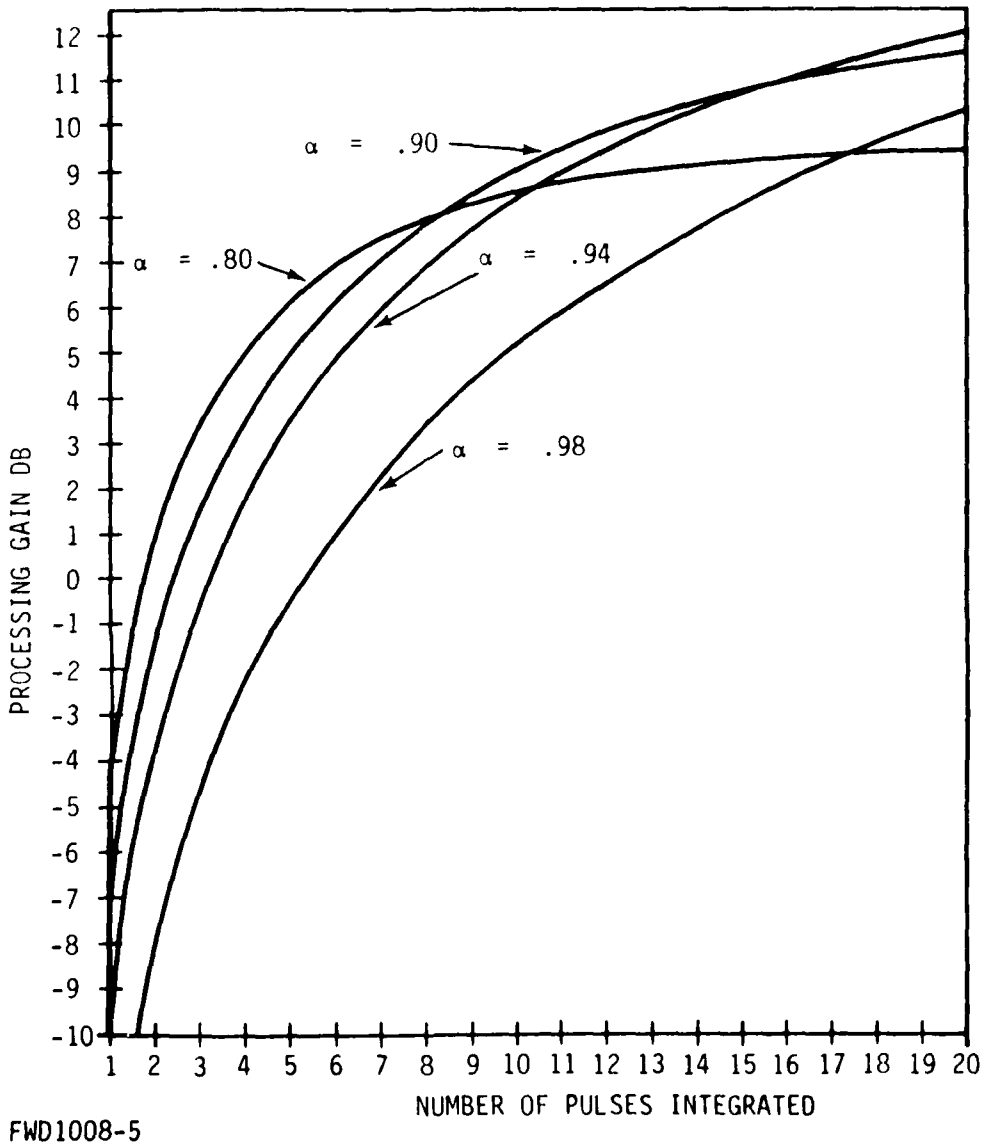
But $\dfrac{s^2(t)}{\bar{n}^2}$ is just the input signal to noise ratio to the Recirculating Integrator, hence the processing gain provided by the Recirculating Integrator is

$$PG = \frac{(SNR)_0}{(SNR)_{in}} = \frac{(1-\alpha^N)^2\ (1+\alpha)}{(1-\alpha)}. \qquad (5)$$

Equation (5) is plotted in Figure 6 as a function of N, the number of pulses integrated, for various values of loop gain. Note that the Recirculating Integrator does not provide any processing gain for the first few pulses; in fact, it degrades the signal to noise ratio by

---

*In this situation the net loop gain must be less than unity for stable operation of the Recirculating Integrator. Stable operation can be obtained for loop gains equal to or greater than unity if the feedback path is periodically opened, but this would imply apriori knowledge of the time of arrival of the sync sequence which of course is not the case in this application.



FWD1008-5

Figure 6. Recirculating Integrator Processing Gain Vs. Feedback Ratio

an amount dependent upon α. However, after a few pulses the Recirculating Integrator processing gain grows at a rate inversely related to the value of α.

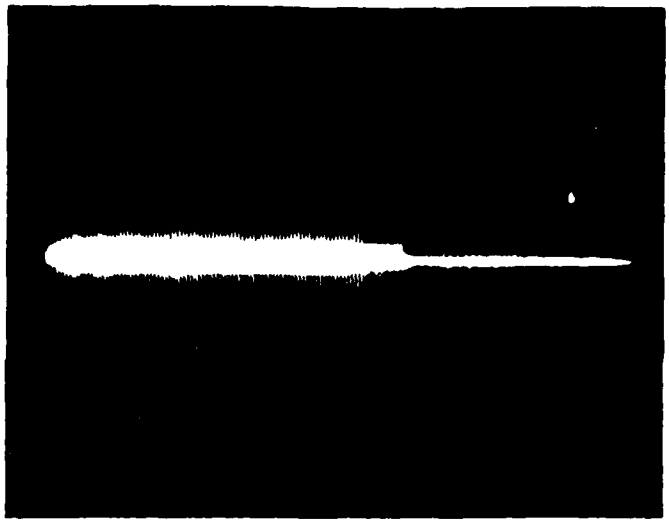
For a net feedback loop gain α of 0.9, the initial Recirculating Integrator processing gain is -7.2 dB and the processing gain for 20 pulses integrated is 11.7 dB. This represents an increase in Recirculating Integrator signal output of about 18.9 dB over 20 pulses. By equation (3), the steady state noise power output grows 7.2 dB which is to be expected since this is the initial processing gain degradation predicted by equation (5). A net loop gain of 0.9 implies that the feedback loop gain must be approximately 54 dB. Therefore, at the output of the loop gain amplifier, or equivalently, at the feedback input to the Recirculating Integrator, the initial signal and noise components can be considered at -17.1 dBm and -24.4 dBm respectively as shown in Figure 5. Hence, the signal to noise ratio for the first correlation pulse processed by the Recirculating Integrator is +7.3 dB. After 20 correlation pulses are processed, the signal component grows 18.9 dB to approximately +1.8 dBm and the signal to noise ratio is +26.2 dB. This represents a theoretical maximum system processing gain of 42.2 dB*, (for a -15 dB input SNR and 1 dB limiter loss), as compared to the theoretical maximum 44 dB predicted by the time-bandwidth product of the sync signal.

As noted above, the signal component varies 18.9 dB at the output of the Recirculating Integrator throughout the build-up cycle for a signal to noise ratio of -15 dB at the link receiver input. The equivalent signal component variation at the input to the Recirculating Integrator can be expected to vary a maximum of about 16 dB as the signal-to-noise ratio improves because of the action of the receiver AGC and limiter as described previously. This implies that the Recirculating Integrator loop gain amplifier would have to be capable of supplying a peak power of +18 dBm in the high signal to noise ratio case if some sort of sync processor ALC were not included. However, ALC is incorporated in the design of the sync processor such that the peak linear output power supplied by the feedback gain need be no more than +10 dBm which is well within the capabilities of present day off-the-shelf amplifiers. The sync processor ALC control is incorporated with the sync detector logic processing and will be described in the sections to follow.

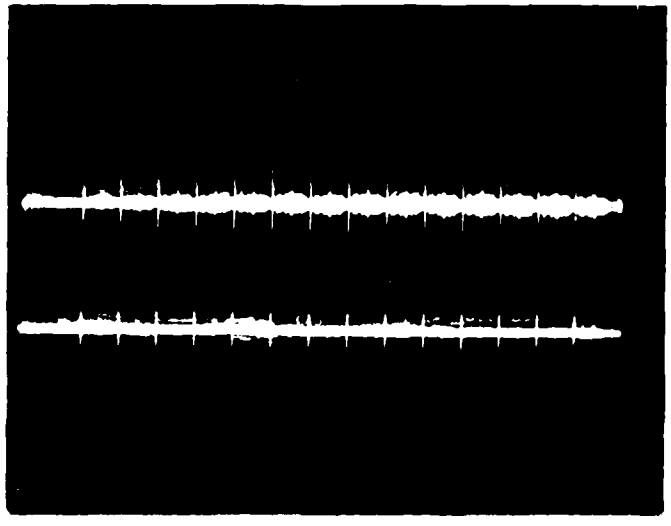
The operation of an experimental surface wave device Recirculating Integrator processing the correlation pulses produced by a surface wave device PSK matched filter is shown in Figure 7. In this example, the matched filter, fabricated on ST Quartz, operates at an 85 MHz center frequency and is matched to a 127 chip maximal linear sequence clocked at a 10 M chip/sec rate. The Recirculating Integrator delay line, also fabricated on ST Quartz, is designed for an approximate "brick-wall" band width of 13 MHz, and the time delay of the Recirculating Integrator is 12.7 μs. As can be seen in Figure 7(a), when the matched filter is periodically excited by the PN-PSK signal that it is "matched" to, the

---

*The factors which degrade theoretical performance are discussed in the system performance section to follow.



(a)



(b)

FWD1008-21

Figure 7. Experimental Recirculating Integrator Response

output of the Recirculating Integrator grows exponentially to a steady state value and then decays to zero once the input signal to the matched filter is removed. Figure 7(b) illustrates the input/output characteristics of the Recirculating Integrator shown in Figure 7(a). The lower trace in Figure 7(b) shows the constant amplitude, periodic output of the 127 chip surface wave device PSK matched filter and the upper trace shows the beginning of the Recirculating Integrator build-up cycle.

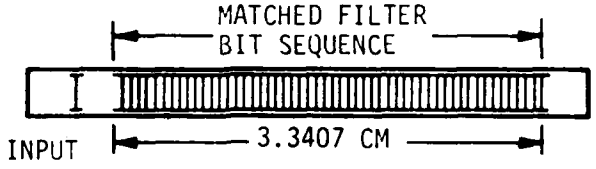
5.3.2 Surface Acoustic Wave (SAW) Devices

5.3.2.1 Device Requirements. - Two specific types of SAW devices are required for implementation of the sync processor. The sub-sequence matched filters (SSMF) recompress the energy contained in the transmitted PN sequences to give a high resolution time domain correlation pulse. The correlation pulses from each of the six SSMF units are coherently added on the Recirculating Integrator Delay Line (RIDL) and the resulting waveform is fed back to the input of the RIDL to be coherently added to the next sequence of correlation pulses from the SSMF's. The geometry for the required devices is sketched in Figure 8. The SSMF inputs on the RIDL are labeled A through F on the figure and the circulated input is labeled CI.

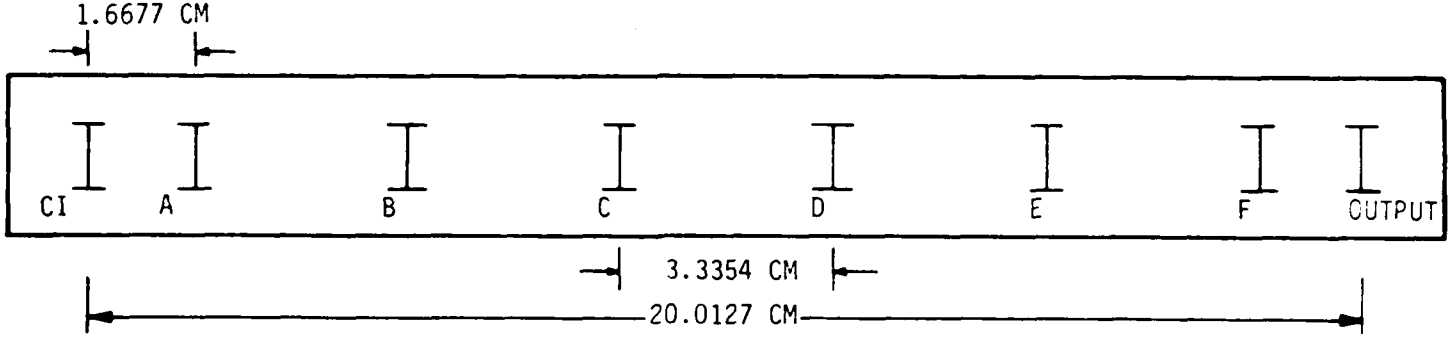
The specific requirements of each of the devices are complied in Table 5-1. Realization of the SSMF's is a straightforward task requiring a moderate amount of care in fabrication. ST-cut Quartz is proposed for the substrate material for temperature stability and minimization of acoustic reflections in the long coded transducers. The most critical parameter is the variation in delay time between devices. This causes phase errors which degrade the coherent summation process and thus the peak value of the correlation pulse at the RIDL output transducer.

Realization of the RIDL will be considerably more difficult, due primarily to the fine tolerances required and its length. The most critical parameter is variation in the delay time between the RI input and the output. An analysis indicated that this delay must match the period of the 1250 chip code sequence to within 0.1 nanosecond to prevent degradation of the processing gain in excess of 1 dB. This represents a delay variation of less than 1.5 parts per million over the operating temperature range. In order to achieve this stability a rotated ST-cut quartz is proposed which exhibits a vanishing first order temperature coefficient of delay at 65°C. This allows excellent delay stability by placing the RIDL in an oven enclosure at a temperature stabilized well above laboratory ambient.

5.3.2.2 Phase Errors. - The processing gain of the sync processor is severely degraded by phase errors in the SAW devices. These errors can be directly attributed to errors in delay times caused by uncertainties in electrode positions and in the SAW velocity. Positional accuracy is dependent on the methods used to produce the final artwork from which transducer electrodes are contact printed. Velocity variations are caused by variations in crystal orientation of the substrate and alignment of the transducer patterns with crystalline axes.



SUBSEQUENCE MATCHED FILTER



FWD1008-10

RECIRCULATING INTEGRATOR DELAY LINE

Figure 8. Device Geometry

Table 5-1. Key SAW Device Requirements

A. Subsequence Matched Filters (SSMF)

Center frequency	137.8 MHz
Chip rate	19.69 MHz
Block length	208 chip (5) 210 chip (1)
Modulation Format	Biphase
Total length	1250 chips (6 blocks)
Delay variation between blocks	0.5 nsec
Substrate material	ST-quarts (42.75° rot. Y-cut)
SAW velocity	3.157 (10^5) cm/sec

B. Recirculating Integrator Delay Line (RIDL)

C nter Frequency	137.8 MHz
Delay time requirements:	
F to output	5.292 usec ±0.4 nsec
E to output	15.874 usec ±0.4 nsec
D to output	26.456 usec ±0.4 nsec
C to output	37.038 usec ±0.4 nsec
B to output	47.619 usec ±0.4 nsec
A to output	58.201 usec ±0.4 nsec
CI to output	63.492 usec ±0.1 nsec
Bandwidth 0.3 dB	20 MHz
3 dB	30 MHz
Peak in-band ripple	0.1 dB
Shape factor	Not critical
Ultimate rejection	35 dB
Substrate material	37.14° rot. Y-cut quartz
SAW Velocity	3.152 (10^5) cm/sec

For ST-cut quartz, the fractional variation in the SAW velocity with orientational errors is given by

$$\frac{\Delta v}{v}_{\text{orientation}} = (343\delta + 99\theta^2 + 58\psi^2) \times 10^{-6}$$

where

δ = deviation from ST-cut Y-rotation angle of 42.75°

θ = angle between X axis of crystal and the surface plane

ψ = angle between X axis of projection on the surface and the propagation direction.

(All angles in degrees)

Errors in transducer alignment are described by the angle ψ above, thus

$$\frac{\Delta v}{v}_{\text{alignment}} = 58\psi_a^2 \times 10^{-6}$$

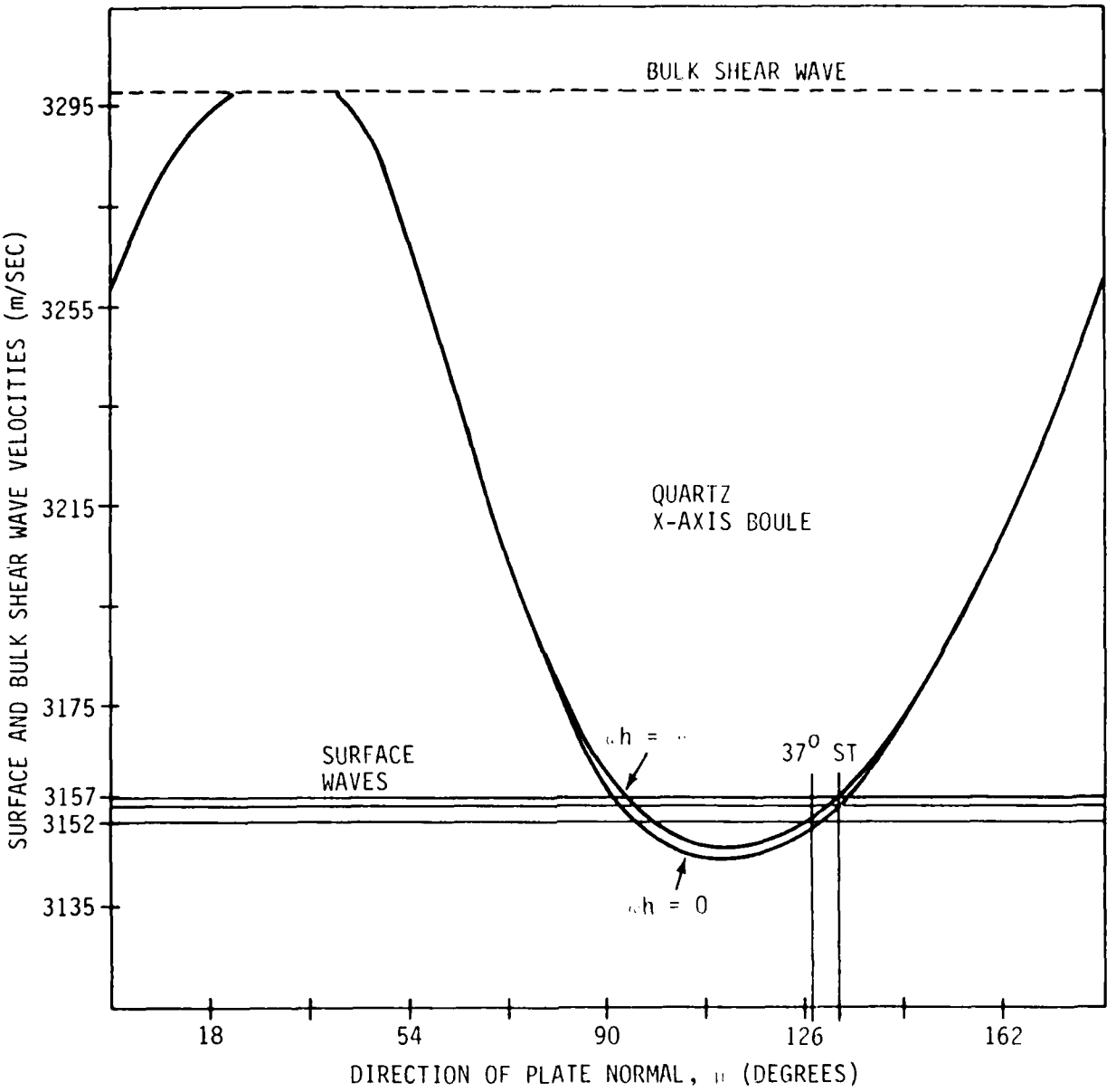
where ψ_a is the alignment error in degrees.

Since the delay accuracy specified for the SSMF units relates maximum delay error between units, it is apparent that the optimal approach is to plot the artwork for all six devices simultaneously. Fabrication is then accomplished with a single photolithographic process on a suitably sized substrate. Delay errors are then due to plotter errors which are negligible.

Considerably more effort is required to meet the delay tolerance required of the RIDL. The worst case condition is given by the 0.1 nsec tolerance required between the RI input and the output transducer. This corresponds to a fractional tolerance $\frac{\Delta\tau}{\tau}$ of approximately 1.6 (10^{-6}). Since $\tau = \frac{\ell}{v}$, $= \frac{\Delta\tau}{\tau} = \frac{\Delta\ell}{\ell} - \frac{\Delta v}{v}$.

A high degree of accuracy in the placement of the transducers can be obtained using laser interferometer controlled step and repeat facilities which are obtainable from a number of vendors. Utilizing this technique an accuracy of 1 μm in the placement of transducers separated by approximately 20 cm yields a fractional accuracy of $5(10^{-6})$.

The accuracy in the value of the SAW velocity depends on the orientation and alignment accuracies noted above. Figure 9 illustrates the dependence of the SAW velocity on the direction of the plate normal for X-axis propagation on quartz. Note that the velocity of the 37° rotated Y cut proposed for the RIDL substrate is very near that of the



NOTE: SURFACE WAVE TIME AVERAGE POWER FLOW ANGLE IDENTICALLY ZERO FOR BOTH h = AND h = 0.

FWD1008-12

Figure 9. Surface Wave Velocity Vs. Direction

ST cut, thus we apply the equation presented previously for the fractional velocity variation to obtain

$$v\ (37.14^{o}\ \text{cut}) = 3.152\ (10^{5})\ \text{cm/sec}$$

Assuming orientational accuracy of 0.25^{o} (15 min.) for all angles (per vendor quotation) yields a fractional velocity tolerance

$$\frac{\Delta v}{v} = 95.6\ (10^{-6}).$$

Alignment errors are expected to be negligible due to the length of the pattern. An alignment line can be included on the artwork which will be aligned with the edge of the crystal. An error of 1mm along the 20 cm length corresponds to an error ψ_a of approximately 0.3^{o} yielding an additional $\frac{\Delta v}{v}$ of $5.2\ (10^{-6})$. In practice, maintaining errors to less than 1mm is easily achievable.

The fractional velocity tolerance dictated by orientational accuracy corresponds to a delay tolerance of 6.1 nsec. Thus, a means of delay compensation is required to adjust the final value to within the specified limits. A two step process is proposed in which the initial design is accomplished with delays specified approximately .01% below the design goal. After fabrication and testing a first order correction is made based on experimental measurements by evaporating aluminum strips on the surface of the RIDL between transducers. This causes a decrease in the SAW velocity of approximately 0.07% in the metallized regions with a resulting increase in delay. (Film thickness of 400 - 600 Å exhibit sufficient conductivity to effect a velocity perturbation without causing significant dispersion due to mass loading.) It is anticipated that fine adjustment to within 1 nsec of the desired delay is realizable with this technique. Final trimming of delay times is then possible using short lengths (<1 meter) of coaxial cable.

5.3.2.3 Device Design. - Design of the SSMF transducer patterns is straightforward. One finger pair per chip is used in the code sequence in order to minimize interelectrode reflections. The input transducer consists of seven finger pairs. On ST-quartz the SAW wavelength at the center frequency (137.8 MHz) is 22.9 μm, thus, finger widths are 5.7 μm. A beamwidth of 75 wavelengths allows all six SSMF patterns to be plotted on one piece of film for simultaneous fabrication. A drift space corresponding to a delay of approximately 1 μs is included between transducers to minimize direct coupling. The fractional bandwidth of each SSMF is approximately 15% and an insertion loss of approximately 50 dB is expected on the basis of predicted input impedance and anticipated parasitic capacitances.

The desired frequency response for the RIDL is sketched in Figure 10 and represents an approximation to the ideal "brick wall"

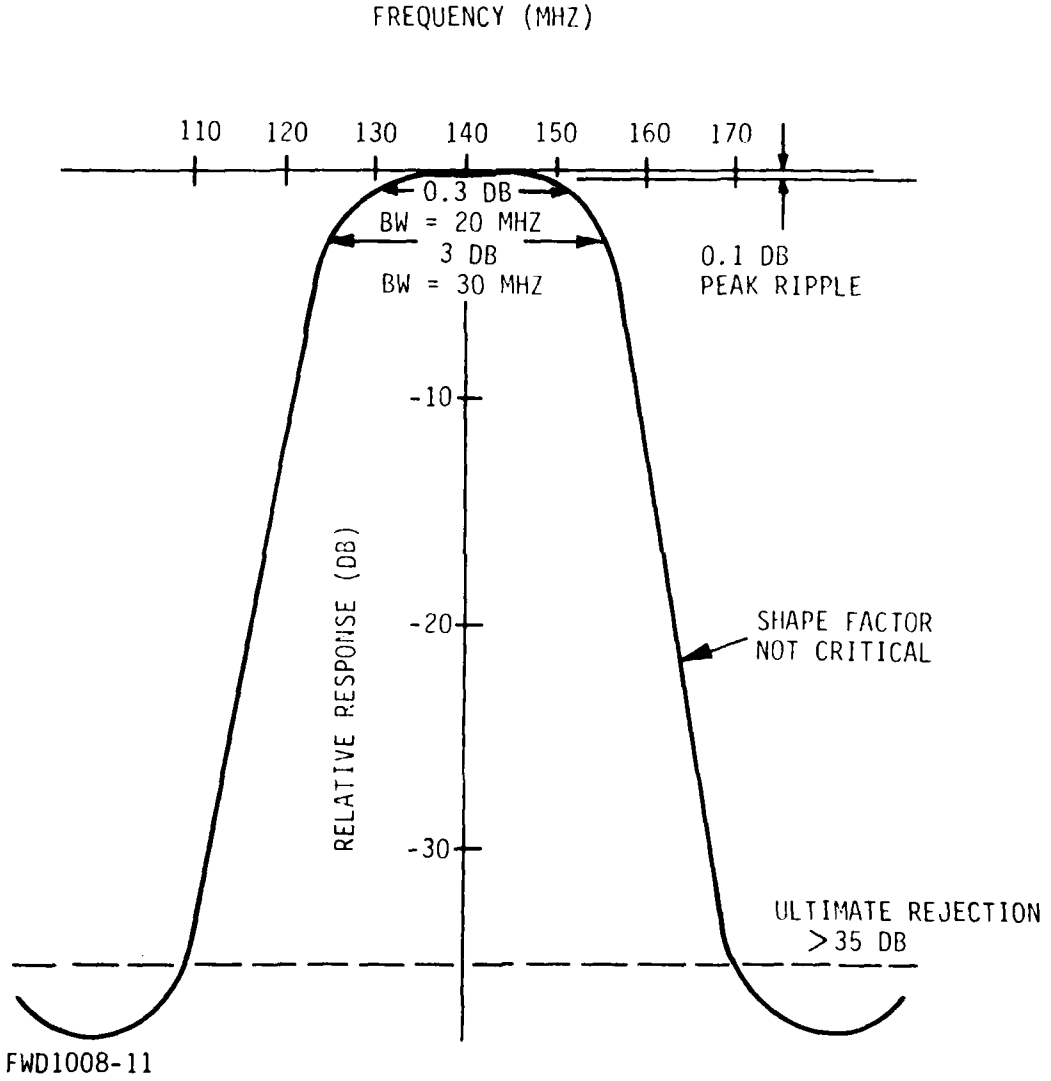


Figure 10. Desired Reponse of the Recirculating Integrator

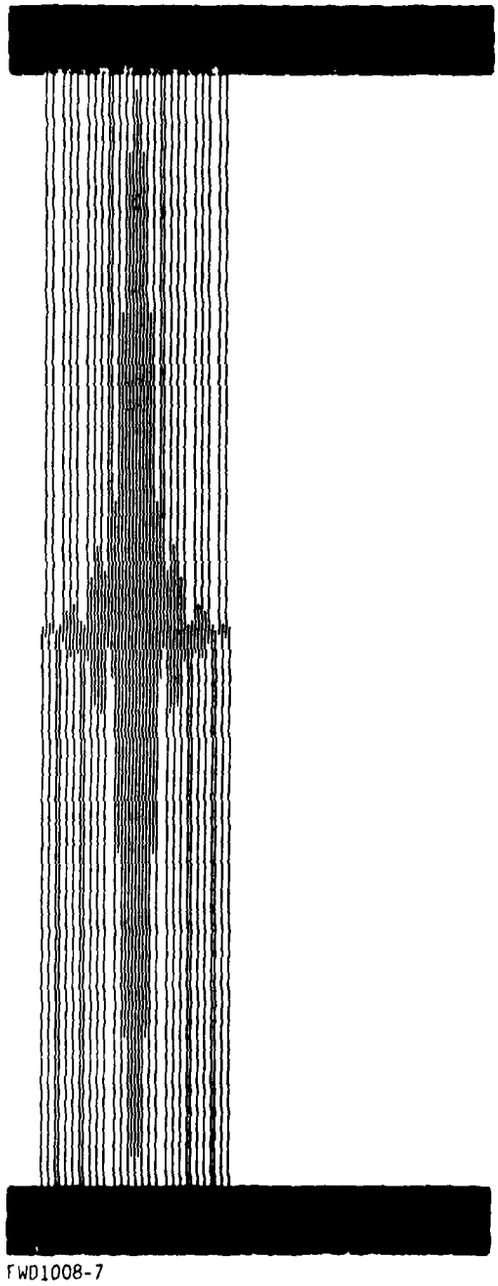
response to minimize loss in processing gain due to band limiting during successive recirculations of the signal. The amplitude ripple specified results in less than 1 dB ripple after ten circulations. Usual design techniques involve a single apodized transducer to give the desired response in conjunction with a wide band unapodized transducer. It is anticipated that this approach would result in excessive insertion loss. Thus, it is proposed that each of the transducers in the RIDL structure be weighted. In particular, the output transducer is weighted using the standard overlap technique as illustrated in Figure 11 while each of the input transducers (labeled R1, and A thru F in Figure 8) are weighted using the capacitive division technique illustrated in Figure 12. Finger widths and spacing will be nearly identical to that used in the SSMF transducers. Diffraction of the SAW beam is typically responsible for ripples in the phase response of filter structures. This results in variations in the effective delay time with frequency and could cause degradation in the processing gain of the RIDL. A beamwidth of approximately 150 wavelengths minimizes these effects by ensuring that any transducer is in the acoustic "far field" region of all other transducers, while resulting in less than 2 dB additional insertion loss due to beam-spreading. The predicted response of the overlap weighted transducer is shown in Figure 13, that of the capacitively weighted array in Figure 14 and the composite response in Figure 15.

A prototype delay line centered at 112 MHz has been constructed and is composed of one each of the transducers illustrated in Figures 11 and 12. The measured response of the prototype is shown in Figure 16 and generally corresponds favorably to the predicted response. The response is degraded by sidelobes which are attributed to diffraction effects and bulk mode propagation. The measured insertion loss is 48 dB which is an acceptable figure based on the maximum value of 55 dB assumed in the previous discussion concerning system operation.

In addition there exists approximately 0.5 dB of passband ripple attributed to uncompensated phase errors and interelectrode reflections in the output transducer. (The fine-grained ripple in the response in Figure 16 is an artifact of the measurement technique.) It is anticipated that these sources of error can be successfully compensated or eliminated in further iterations of the design process.

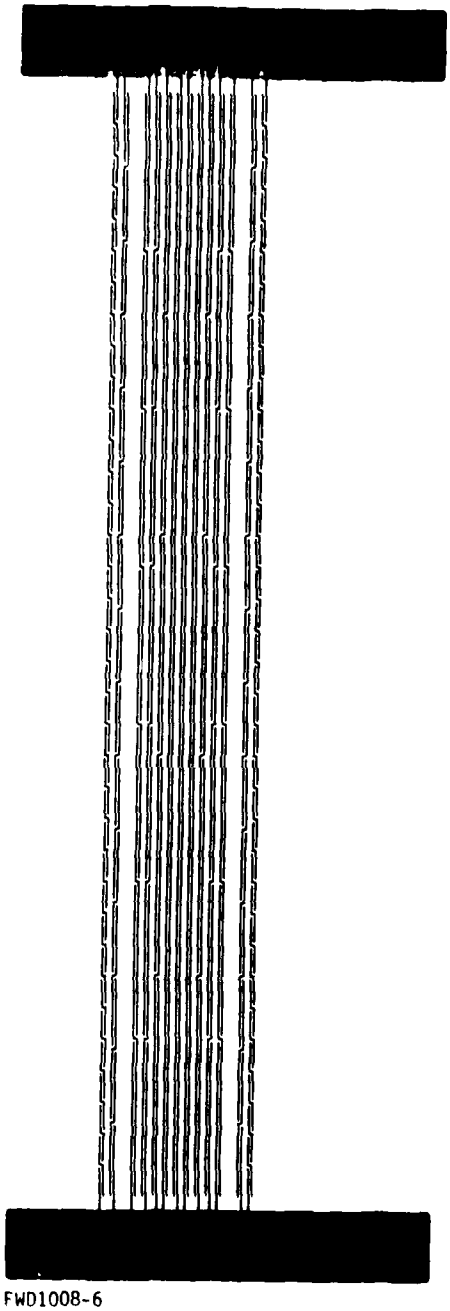
5.3.2.4 Fabrication and Packaging Techniques. - All of the SAW devices required in the sync processor can be fabricated using standard photolithographic techniques. Due to the delay tolerances and size of the RIDL, it will be necessary to produce the artwork on a laser interferometer controlled step-and-repeat system.

The SSMF's will be separated and individually packaged in standard microcircuit packages. Temperature control is not anticipated.



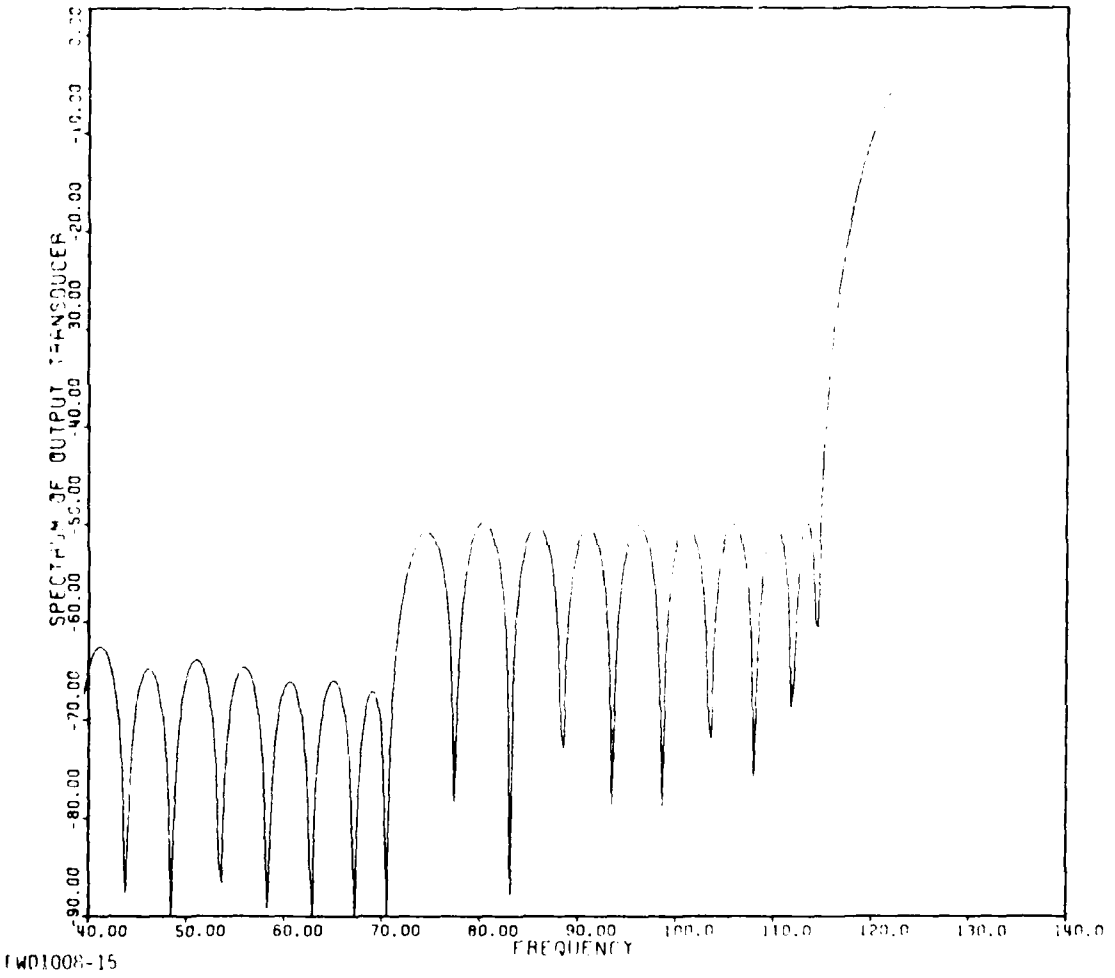
FWD1008-7

Figure 11. Recirculating Integrator Output Transducer



FWD1008-6

Figure 12. Recirculating Integrator Input Transducer



FWD1008-15

Figure 13. Spectrum of Output Transducer Versus Frequency

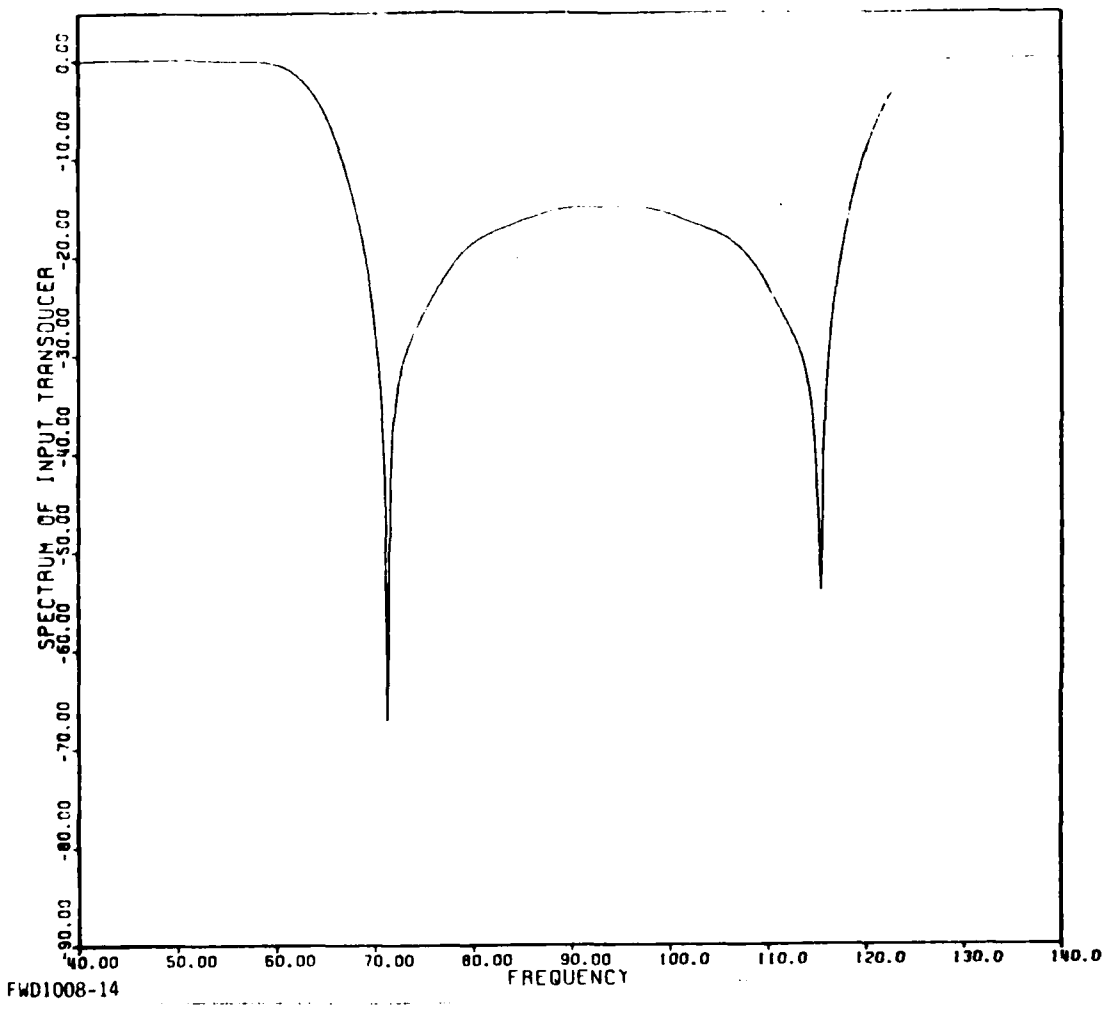


Figure 14. Spectrum of Input Transducers Versus Frequency

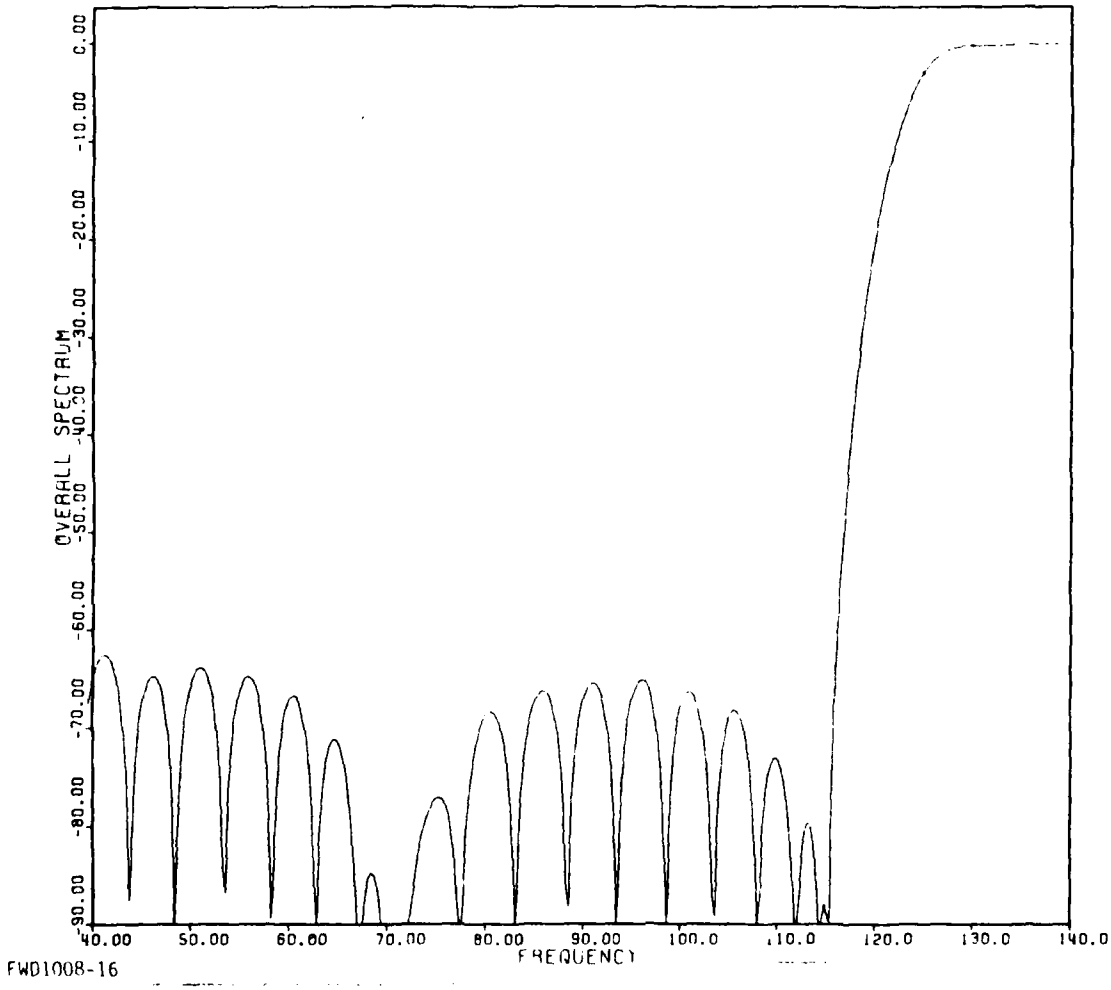


Figure 15. Overall Spectrum Versus Frequency

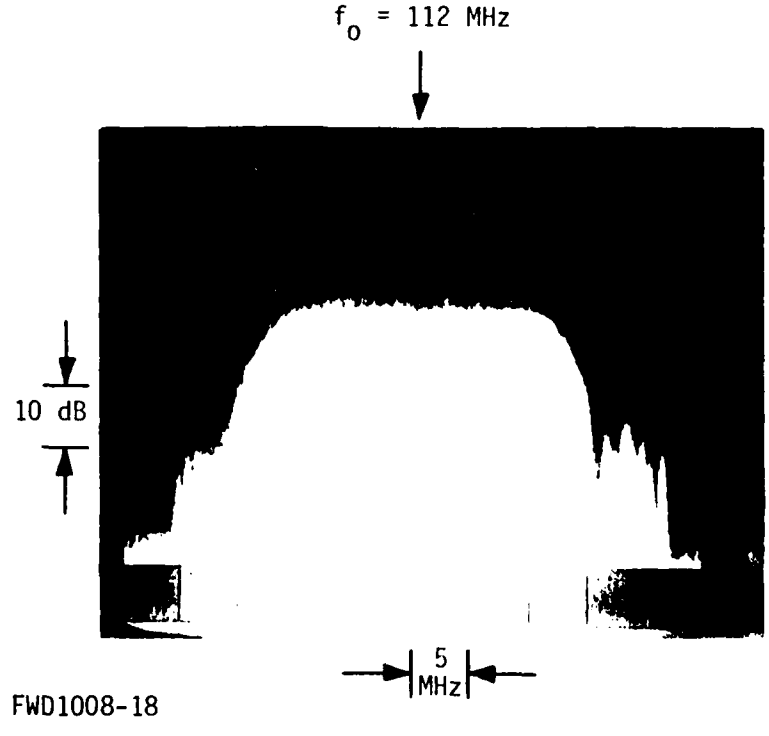


Figure 16. Measured Response of the Prototype Delay Line

The delay tolerance of the RIDL requires that it be mounted in a stable thermal environment. The variation in delay $\frac{\Delta\tau}{\tau}$ for the 37.14° rotated Y-cut of quartz is plotted in Figure 17 as a function of $T - T_{to}$, where T_{to} is the "turn over" temperature, (65°C). Of particular concern is the generation of a temperature gradient along the length of the substrate. The horizontal line on the diagram give the range of mean temperatures over which the specified variation will result in acceptable delay tolerance. Note from the figure that if the mean temperature of the substrate is stabilized to within ±2°C of T_{to}, a 5°C gradient over the length of the substrate will cause a time delay error of less than the required 1.5 ppm.

It is proposed that the RIDL substrate and corresponding matching networks be mounted in a temperature controlled enclosure as illustrated in Figure 18. The surface of the surface wave delay line will be maintained at a constant temperature of 65°C ±1°C by the use of a foil type flexible heater which is placed in intimate contact with the back side of the surface wave device. Because of the very low mass, this heater will generate heat almost instantaneously and because of the foil construction the heat will be uniform over the entire surface. The foil heater can be either ruggedized stranded resistance wire in a layer of insulating material or chemically etched from metal foil laminated to a base insulation.

A precision thermal sensor is attached to the face of the surface wave delay line and provide outputs to a custom designed electronic controller which will maintain the 65°C ±1°C surface temperature. Requiring 28 Vdc input power to the thermal controller module, the foil heater will consume approximately 11 watts max power using a proportional voltage technique. The thermal controller itself will dissipate approximately 7 watts.

5.3.3 Sync Pulse Detector and Sync Detector Logic

5.3.3.1 General Discussion. - The signal at the output of the Recirculating Integrator is a 138 MHz carrier which is amplitude modulated by the sync pulses and Rayleigh-distributed noise plus sidelobes from the PN sequence. This signal is detected using an envelope detector and matched filter to produce a baseband signal plus noise. The matched filter is chosen to maximize the baseband SNR to within practical limits determined by the complexity of the filter. Since the signal is deterministic and the noise statistics are defined, performance to within 1 dB of an optimum detector matched filter can be readily achieved. Also, since the worst case SNR at the input to the envelope detector is approximately +7 dB for a received signal to noise ratio of -15 dB (and increases rapidly due to the RI processing gain), the degradation in overall performance for the envelope detector relative to a perfect synchronous detector is less than 1 dB.

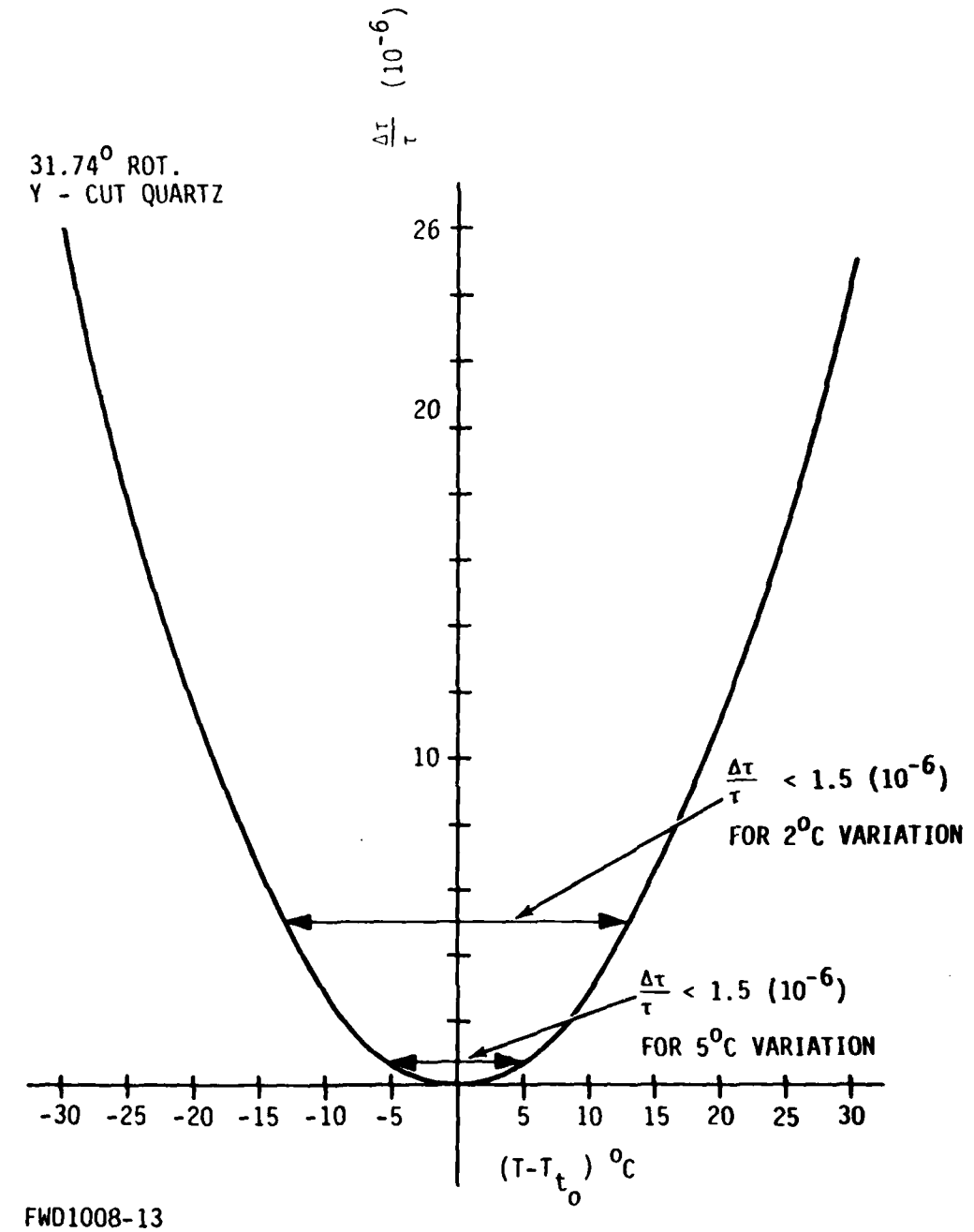


Figure 17. Time Delay Vs. Temperature

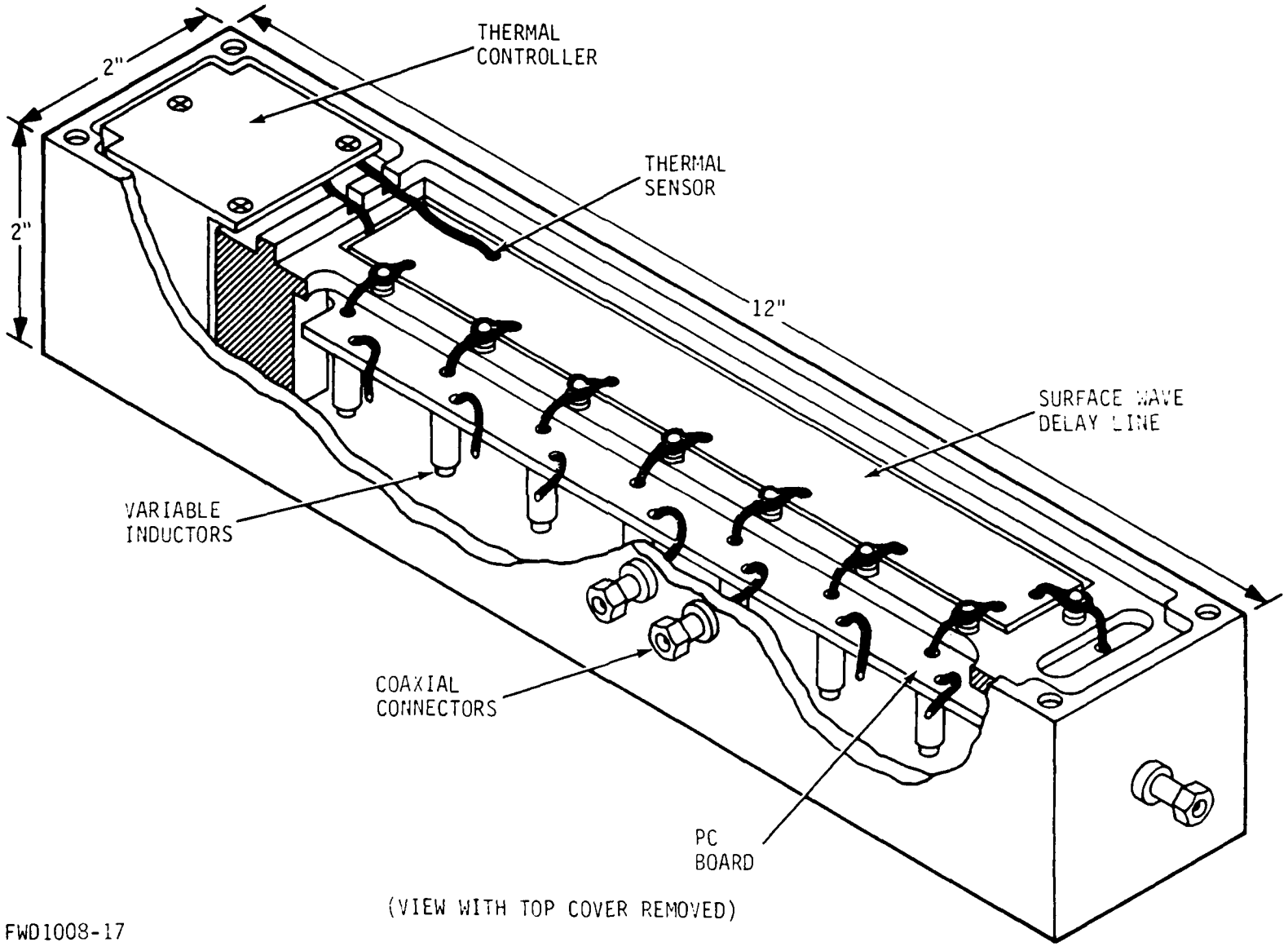


Figure 18. Recirculating Integrator Mechanical Layout

The envelope detector/matched filter output is applied to the input of a Tracking Threshold Detector (TTD) which produces uniform 50 nanosecond pulses for the Sync Detector Logic. The Sync Detector Logic utilizes an algorithm (described below) to discriminate between TTD outputs due to bonafide signal pulses and noise pulses. Once the algorithm "locks on" to the sync signal pulses it tracks them for several lines. Each time a "good" sync pulse is recognized an accumulator is incremented. When a noise pulse is detected the accumulator is decremented. When the accumulator reaches a predetermined number of counts the probability that good sync has been obtained is practically unity. At this point the output sync pulses are phase shifted to correspond to the newly determined sync phase and remain at this phase until the process is repeated.

From the above description, the operation of the TTD and the sync pulse processor logic are closely related, particularly for low detector SNR (weak input signals). In fact the TTD performance can be optimized (in theory) to maximize the probability of achieving sync under all SNR conditions. In reality, however, this optimization of the TTD performance is not as critical as might be expected for two reasons: (1) At low (e.g., 6-7 dB) SNR the probability of achieving sync, although maximized, is too low (<0.1) to be of any practical interest*, and (2), the probability of achieving sync at high (e.g., > 14 dB) SNR approaches unity very rapidly with a corresponding increase in the range over which the TTD performance is "optimum".

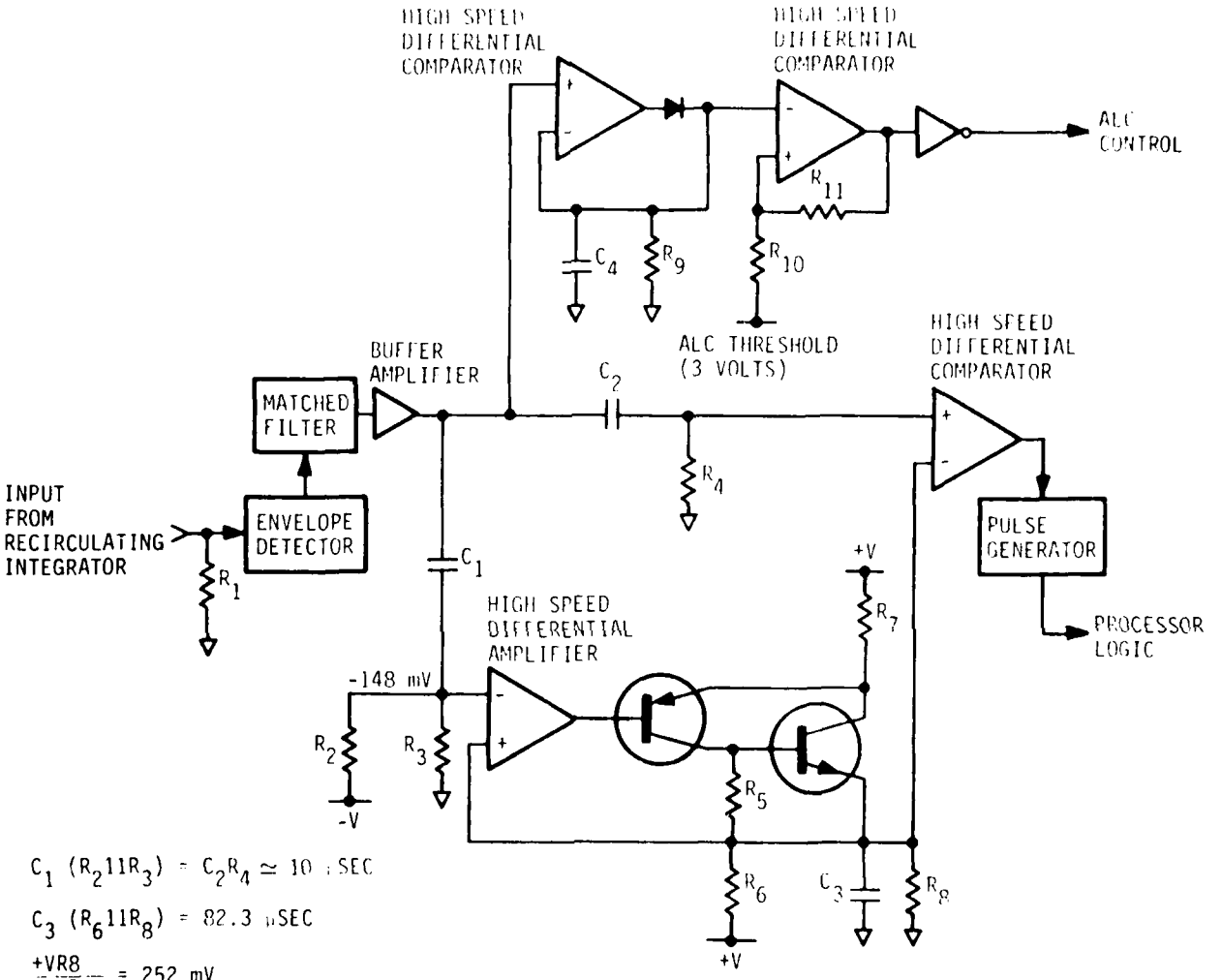
5.3.3.2 Tracking Threshold Detector. - The general design of the Tracking Threshold Detector is shown in Figure 19. The TTD consists of a high speed differential comparator which outputs a logic "one" whenever the "+" input level (signal) exceeds the "-" input (reference). The reference or decision level, B, is the TTD parameter which is optimized to maximize the probability of achieving sync for a given SNR. If B is set too high then the probability of missing the signal, P_m, increases. If B is set too low then the probability of a flase alarm, P_f, increases. As will be shown below, maximizing the probability of achieving sync is equivalent to maximizing the expression

$$(1 - P_m)^2 \ (1 - P_f)^{1249} = f(B, SNR)$$

with respect to B. This expression results from the operation of the sync processor logic and can be maximized by setting $\frac{df}{dB}$ to zero and solving for B. To do so requires functional relationships for P_m and P_f in terms of B and SNR. Since the noise at the envelope detector output is Rayleigh distributed, the signal plus noise will be Rician distributed. For the noise case the probability density function is given by:

---

*Actually the probability approaches zero due to provisions in the algorithm for avoiding false sync acquisitions.



$C_1 (R_2 \| R_3) = C_2 R_4 \simeq 10$ μSEC

$C_3 (R_6 \| R_8) = 82.3$ μSEC

$\frac{+VR8}{R_6+R_8} = 252$ mV

$C_4 R_9 \simeq 600$ μSEC (ALC TIME CONSTANT)

FWD1008-24

Figure 19. Tracking Threshold Detector

$$P_n(r) = \frac{r}{\sigma_n} e^{-\frac{r^2}{2\sigma_n^2}},$$

where σ_n is the variance of the function and equals the RMS noise voltage. P_f, the false alarm probability, is the area of $P_n(r)$ above B:

$$p_f(r) = \int_B^\infty P_n(r)dr = e^{-\frac{B^2}{2\sigma_n^2}}.$$

For the signal case the probability density function is given by

$$p_s(r) = \frac{r}{\sigma_n^2} e^{-\frac{r^2+A^2}{2\sigma_n^2}} I_o\left(\frac{rA}{\sigma_n^2}\right)$$

where A is the peak signal (sync pulse at output of the envelope detector) voltage and $I_o(x)$ is the modified Bessel function of the first kind and zero order. P_m, the probability of missing a signal pulse, is the area of $P_s(r)$ below B:

$$P_m = \int_o^B p_s(r)dr.$$

This last expression cannot be represented in closed form, but it can be approximated very closely:

$$P_m \simeq \frac{1}{2}\,\mathrm{erfc}\left(\frac{A-B}{\sigma_n\sqrt{2}}\right) \simeq \frac{\sigma_n}{A-B}\sqrt{\frac{2}{\pi}}\, e^{-\frac{(A-B)^2}{2\sigma_n^2}}$$

for $\frac{A-B}{\sigma_n} >> 1$, i.e., "large" SNR.

Substituting the above expression for P_f and P_m into the original equation and differentiating:

$$\frac{df}{dB} \simeq e^{\frac{AB}{\sigma_n^2} - \frac{A^2}{2\sigma_n^2} - \ln 1249\sqrt{\frac{\pi}{2}}} - \frac{B}{\sigma_n} \to 0, \quad \frac{A}{\sigma_n} \geq 7$$

where the SNR equals $20 \log \frac{A}{\sigma_n}$.

The solution of this equation, normalized to σ_n, is approximately a straight line with the equation:

$$\frac{B_{opt}}{\sigma_n} = 0.462 \frac{A}{\sigma_n} + 1.346, \quad \frac{A}{\sigma_n} \geq 7.$$

For low SNR $\frac{B_{opt}}{\sigma_n} \rightarrow 3.776$; however, as stated above, the probability of acquiring sync at low SNR becomes small due to the provisions in the sync processor algorithm for protecting against false sync.

Referring again to Figure 19, the output of the envelope detector matched filter is applied to three separate circuits. The first, through C_2, is to the pulse comparator referred to above. The purpose of C_2/R_4 is to remove any dc component which might appear on the signal due to CW interference. The effect of this filtering is to translate the signal plus noise by an amount $\sigma_n\sqrt{\frac{\pi}{2}}$ * in the negative direction but this offset is compensated in establishing the decision threshold.

The signal path through C_1 is to the threshold determining circuit. The high speed differential amplifier and two transistors function as a peak detector. The input signal is offset by 148 mV by R_2/R_5 and compared with the peak detector output which appears across $C_3/R_6/R_8$. When the offset input signal peak exceeds the peak detector output voltage (equivalent to B referred to above) a 100 mA current is driven into C_3 which charges to the value of the input voltage. When the input signal returns to the noise floor C_3 discharges through R_6/R_8 to a 252 mV level with an 82.3 μs time constant. The time constant and levels were chosen to produce a detector threshold of

$$\frac{B_{opt}}{\sigma_n} - \sigma_n\sqrt{\frac{\pi}{2}}$$

volts after 63.492 μs. In this manner the detector tracks the signal input and provides the optimum decision threshold (as determined above) for the succeeding input pulse.

Note in the preceding discussion that the threshold for a given pulse is set at an "optimum" level based on the pulse before. An implicite assumption with this technique is that all input pulses are of approximately equal amplitude, which, without the buildup of the Recirculating Integrator, is a reasonable one. But with the RI, the pulses do increase in amplitude from one to the next with the amount of increase dependent on the input signal strength, the line number (1-20), the feedback ratio, and the history of the previous RI inputs. To account for

- -

*Throughout this discussion the values were determined assuming a 100 mV RMS noise voltage at the TTD input.

all these factors in setting the threshold would require a considerably more complex circuit than is proposed and in the final analysis would not produce a measureable increase in the overall sync processor performance. Also, for low input levels where setting the threshold is most critical, the RI output buildup occurs primarily in the first 10-12 lines so the detector performance is nearly optimized for the remainder.

The third portion of the tracking threshold detector is shown at the top of Figure 19. This circuit provides an automatic level control (ALC) output based on the amplitude of the detector input signal. ALC is necessary in order to minimize the dynamic range requirements on the RF gain and the tracking threshold detector so that the surface wave devices can be operated at signal levels which avoid noise floor problems.

Gain control of the sync processor (and, also, the link receiver) could be derived if the output of the matched filter were available so that the peak value of the correlation pulses could be followed and used to derive a gain control signal. However, the output of the matched filter is not directly accessible, only the output of the Recirculating Integrator is available and this output grows as a function of time. Therefore, deriving a gain control voltage from the Recirculating Integrator output would be rather complicated, especially if it where desired to control link receiver gain as well as sync processor gain in this manner.

If auxiliary transducers were added to the Recirculating Integrator Delay Line, it would be possible to obtain a signal equivalent to the matched filter output in addition to the normal Recirculating Integrator output and the matched filter output could be used to provide gain control voltages. However, the addition of the auxiliary transducers would significantly complicate the RIDL design and is not really necessary in this situation.

The ALC used in the sync processor employs a simple RF switch at the sync processor input (see Figure 5). In the absence of sync signal this RF switch is turned on and exhibits a nominal insertion loss of 2 dB as shown. If the received sync signal level reaches a value sufficient to cause the envelope detected output of the Recirculating Integrator to exceed 3 volts during the buildup cycle, as can happen for received signal to noise ratios of about -8.5 dB or greater, the ALC is activated.

Referring again to Figure 19, when the envelope detector output exceeds 3 volts, C_4 charges to this value and the input to the second ALC differential comparator (connected as a Schmitt trigger) exceeds the + reference causing the output to go low. This level is inverted to a high logic level that is applied to the RF switch which shuts off the input to the sub-sequence matched filters. The RI output then decreases with a decay factor of α. The ALC time constant, R_9C_4, is chosen to yield a corresponding decrease in the input to the ALC comparator. When

the voltage across C_1/R_9 decreases below the ALC threshold of 3 volts the RF switch is turned on and normal buildup resumes. In this manner the amplitude of the detector input pulses will oscillate about the 3 volt level with an amplitude determined by the amount of input overdrive and the Schmitt trigger hysteresis. Although the resulting fluctuation in detector input pulse amplitudes will result in non-optimum decision thresholds being established, the SNR is so high as these levels that the overall performance is not degraded. The reasons for this approach to the ALC are 1), simplicity over a proportional controlled ALC (or AGC), and 2), to allow linear operation of the matched filter at low signal levels where system optimization is most critical. The ALC proposed here is termed a delayed ALC in that its effect is not seem until the signal-to-noise ratio is large enough so that truncation of the incoming sync sequence no longer matters. A question might arise concerning the need for an ALC of any sort - i.e., why not simply clip the detection signal at 3 volts? Since the detection output pulses are approximately 100 nsec wide near the base, allowing an unchecked buildup in amplitude would cause the apparent position of the large amplitude pulses to move ahead in time relative to small pulses. This apparent shift in position would cause the processing algorithm to treat these large pulses as noise with the net effect of reducing the overall probability of sync pulse detection.

5.3.3.3 Sync Detection Logic. - The last section of the sync processor is the Sync Detection Logic (SDL) shown in Figure 20. The input to this circuit is the 50 nsec pulses from the output of the Tracking Threshold Detector. The SDL checks the spacing between successive input pulses and when a sufficient number of pulses occur with the proper spacing, the phase of a local sync pulse generator is shifted (relative to the local clock) to correspond to the phase of the incoming sync pulses. This phase is maintained until a new set of input pulses pass the logic check at which time the sync pulse generator is reset to the newly determined phase (which may be the same as the previous phase in which case no change is seen at the output).

The considerations which were made in designing the Sync Detector Logic will be discussed briefly. First some terms will be defined or redefined:

P_f is the probability of a false fire or false alarm at the output of the TTD.

P_m is the probability of a missed sync pulse (false dismissal).

P_{s1} is the probability of a successful sync check in one trial.

P_s is the probability of obtaining good sync.

P_{fs} is the probability of obtaining false sync.

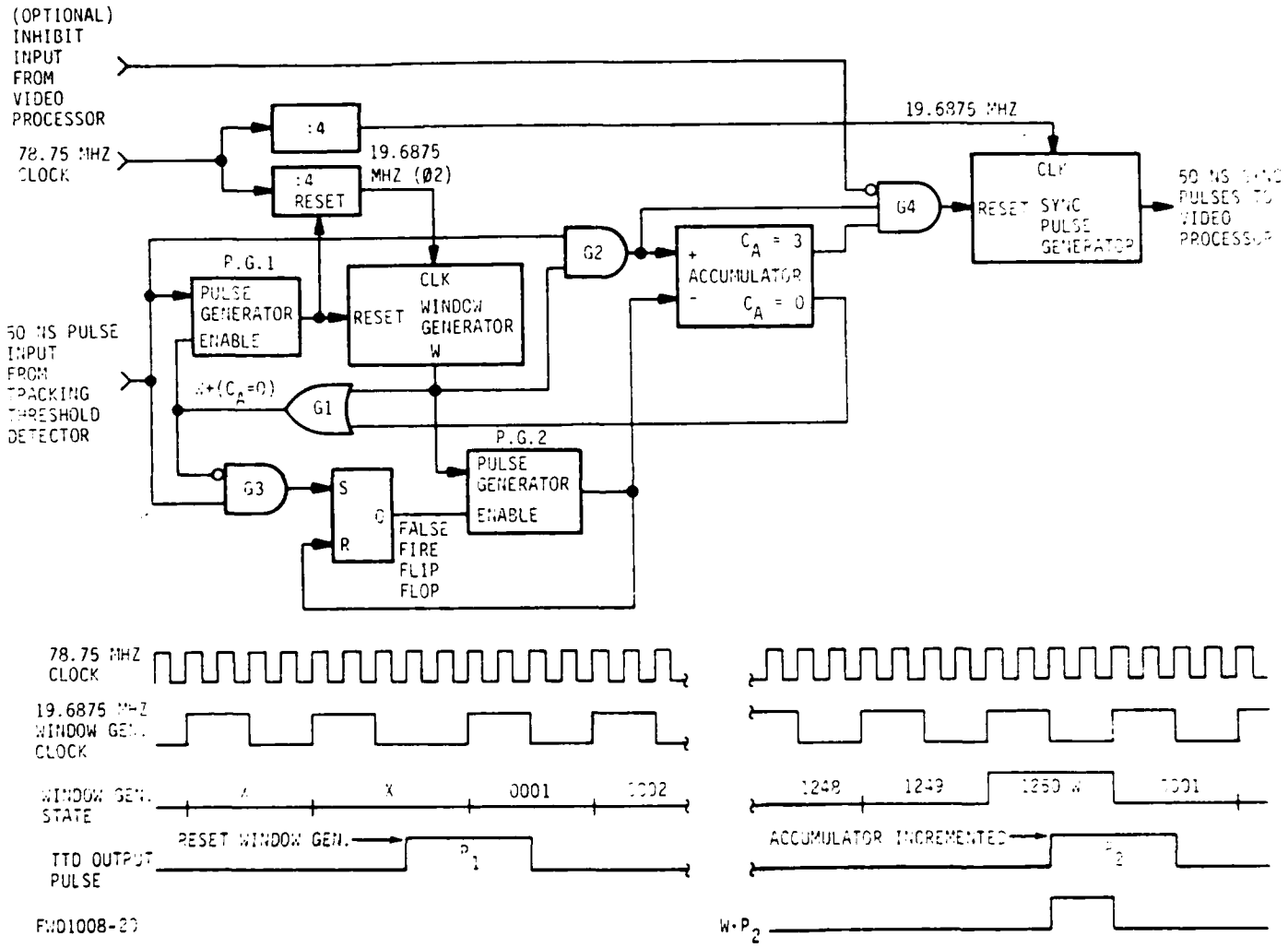


Figure 20. Sync Detector Logic

Of course the goal of the Sync Processor is to maximize P_s and minimize P_{fs} both of which are, ultimately, functions of P_f and P_m (discussed in the previous section). Further, this should be done for as wide a range of inputs as practical and should be oriented towards low SNR conditions since obtaining sync in high SNR conditions is a comparatively trivial problem.

The basic approach used to discriminate between signal and noise pulses is to measure the time between successive TTD outputs and note whether the time interval equals 63.492 μs (±25 nsec). If this occurs, an accumulator is incremented one count. If it does not, and a previous good interval has not been detected, the search is continued. If it does not, and a previous good interval has been established, a mistake, or error, is assumed and the accumulator is decremented one count. When the net contents of the accumulator, C_A, reaches 3 (how the value 3 was chosen will be explained shortly) good sync is presumed and the mod 1250 sync pulse generator is reset by the last "good" TTD output pulse, thereby aligning the phase of the local sync pulses with the received sync signal.

The operation of the Sync Detector Logic can be divided into three modes: 1) search mode, 2) track mode, and 3) lock mode. In the search mode the accumulator count is zero and random pulses due to noise comprise the SDL input. With $C_A = 0$ Pulse Generator 1 is enabled through gate G1 and each input pulse resets the window generator. The window generator output, W, goes high for 50 nsec after 1250 clock times. If a pulse is received in the window, it passes through G2 and increments the accumulator one count and "$C_A = 0$" goes low. The SDL is now in the track mode. If a noise pulse enters the SDL input before the next window arrives, the window counter is not reset since W + ($C_A = 0$) is low but G3 is enabled so the False Fire Flip Flop is set enabling PG2. When the window arrives PG2 is triggered and the accumulator is decremented by one. The count now is back to zero, "$C_A = 0$" is high, and the SDL is back in the search mode.

If a signal is received which, when processed by the sub-sequence matched filters and RI, has sufficient SNR at the TTD to produce detectable pulses, and two good pulses are detected in sequence (i.e., no intervening false fires), the SDL goes to the track mode as before. This time, however, the probability of getting an input pulse in the window due to the signal pulses is high, while, because the TTD threshold level is increasing as the Recirculating Integrator output builds up, the probability of getting false fires is decreasing. Now for each pulse detected in the window an additional count is added to the accumulator. Because of the False Fire Flip Flop one or more pulses between windows will only decrement the accumulator by one. This feature is included to avoid having to start over if a noise burst is received which might otherwise clear out the accumulator.

As soon as the accumulator reaches a count of three, "$C_A = 3$" goes high and enables G4 whose output goes high resetting the sync pulse

generator. The SDL is now in the lock mode. After this action occurs noise may enter and decrement the accumulator, but once the sync pulse generator is reset, correct sync pulse phase (±25 nsec) is established and will remain until the accumulator returns to the search mode and the above process is repeated. Thus, both the window and an excess of three correct-versus-incorrect inputs must be present for the sync phase to be changed.

From the preceding description it is apparent that to transition from the search mode to the track mode there must be two successive inputs spaced 63.492 μs apart. In fact, this condition must be met in order to increment the accumulator, and so is the criteria for success which was previously assigned a probability, P_{sl}. In the presence of a signal where P_f and P_m both have significance, P_{sl} is given as:

$$P_{sl} = (1 - P_m)^2 (1 - P_f)^{1249},$$

i.e., two successive correct pulses must be detected: $(1 - P_m)^2$, and no incorrect pulses detected for 1249 intervals: $(1 - P_f)^{1249}$. It is this quantity that was maximized by the proper choice of B in the TTD.

The probabilities of obtaining correct sync and false sync (P_s and P_{fs}) are seen to be a function of the accumulator threshold given the algorithm described above. Once an optimum B is obtained, however, there is no "optimum" accumulator threshold (optimum in the sense maximizing P_s and minimizing P_{fs}). If N is the threshold of the accumulator then increasing N decreases the chance of random errors resulting in a false sync indication but also puts a more difficult criteria to meet for detecting bonafide sync in the presence of errors. By calculating the above probabilities as functions of N and the line number, L, ($1 \leq L \leq 20$) a tradeoff between acceptably low P_{fs} and adequately high P_s can be made. This determination is done through recursive probability relationships which describe the SDL algorithm.

Given that:

$P_A[+]$ = prob. of accumulator being incremented

$$= (1 - P_m) (1 - P_f)^{1249},$$

$P_A[-]$ = prob. of accumulator being decremented

$$= [1 - (1 - P_s)^{1249}] P_m,$$

$P_A[o]$ = prob. that accumulator is neither incremented nor decremented

$$= 1 - P_A[+] - P_A[-],$$

then,

$$P_L[C_A = n] = \text{prob. that the accumulator has a count of n on line L}$$

$$= P_A[+]\, P_{L-1}[C_A = n - 1] + P_A[o]\, P_{L-1}[C_A = n] + P_A[-]\, P_{L-1}[C_A = n + 1].$$

The probability of obtaining sync on or before the Lth line, $P_L[s]$, if the accumulator must reach a value of N to do so is given by

$$P_{L,N}[s] = \sum_{j=1}^{L} P_j[C_A = N \mid C_A < N,\ j = 1,2,\ \ldots\ L-1],$$

$$P_j[C_A = N] = 0 \text{ for } j = 1,2,\ \ldots,\ N.$$

When L is implied (e.g., L = 20) then $P_L[s]$ is shortened to P_s, the probability of obtaining sync.

The probability of obtaining false sync, P_{fs}, can be addressed for two times of interest: 1) during video processing time (i.e., no sync signal present), or 2) during frame sync time. For the first case the probability of obtaining false sync, $P_{fs}[1]$, can be computed by substituting the quantity P_f for $(1 - P_m)$ in the expressions for $P_A[+]$, $P_A[o]$, and $P_A[-]$ and then computing $P_{L,N}[s]$ as before. The result, $P_{L,N}[fs] = P_{fs}[1]$, has a maximum with respect to P_f which can be determined by differentiating $P_A[+]$, setting the result to zero, and solving for P_f:

$$\frac{dP_A[+]}{dP_f} = \frac{d}{dP_f}\left[P_f\,(1 - P_f)^{1249}\right]$$

$$= (1 - P_f)^{1249} - 1249\, P_f\,(1 - P_f)^{1248} = 0.$$

$$\therefore\ P_f = 8 \times 10^{-4}.$$

Using this value the cumulative probability of false sync was computed for 242 lines (video sub-frame) and for N = 1 through 8.

For the second false sync case (during sync field), $P_{fs}[2]$ can be approximated, for low SNR conditions, by $(P_m)^N P_{fs}[1]$. In this case, however, $P_{fs}[1]$ for the 20th line is used. (Note that $P_{fs}[1]$ for line L is the probability of obtaining false sync on or before line L.)

The probabilities of obtaining correct sync are computed for L = 1, 2, ..., 20; N = 1, 2, ... 8; input SNR of -17.5, -15.5, -12.5, -7.5 dB with the RI, and input SNR of -8, -9, -10, ..., -18 dB without the RI. The worst case (i.e., $P_f = 8 \times 10^{-4}$) false sync probabilities were computed for L = 1, 2, ... 242; and N = 1, 2, ... 8. As expected, P_s and P_{fs} both decrease with increasing N. A partial tabulation of these results is given in Table 5-2.

Table 5-2. Partial Results of P_s and P_{fs} Computations

	N=	1	2	3	4	5
L=1	P_s=	.0233	0	0	0	0
	P_{fs}=	5.86×10^{-4}	8.6×10^{-8}	0	0	0
L=3	P_s=	.3201	.0093	0	0	0
	P_{fs}=	8.8×10^{-4}	2.06×10^{-7}	0	0	0
L=5	P_s=	.9998	.9236	.2864	.0083	0
	P_{fs}=	1.47×10^{-3}	4.81×10^{-7}	1.28×10^{-10}	2.37×10^{-14}	2.17×10^{-18}
L=7	P_s=	1	.9999993	.9998	.9236	.2864
	P_{fs}=	2.05×10^{-3}	7.66×10^{-7}	2.6×10^{-10}	7.53×10^{-14}	1.7×10^{-17}
L=10	P_s=	1	1	1	1	.9999991
	P_{fs}=	2.94×10^{-3}	1.2×10^{-6}	4.68×10^{-10}	1.73×10^{-13}	5.79×10^{-17}
L=242	P_{fs}=	.258	3.45×10^{-5}	1.68×10^{-8}	8.16×10^{-12}	3.97×10^{-15}

Conditions:

$P_{L,N}[s] \equiv P_s$: Input SNR = -12.5 dB, with RI.

$P_{fs}[1] \equiv P_{L,N}[fs]$: No input signal (during video).

Based on these results N = 3 was selected for the Sync Detector Logic parameter. By the end of only 10 lines at an input SNR of -15 dB the probability of obtaining sync is better than seven nines, while at the end of 242 lines of video (no sync signal) the probability of obtaining false sync is less than one in a million. However, since this probability is relatively constant, an input to the SDL is provided to inhibit reset of the sync phase generator during video processing (Figure 20). This provision could be used to reduce the probability of false sync during video to zero. The second case of false sync (i.e., during

a sync interval) has a probability approximated by $(P_m)^N P_{fs}[1]$. For -15 dB SNR and N = 3 this becomes $(B/\sigma_n = 3.776 \Rightarrow P_m = 6.6 \times 10^{-2}$

$$P_{fs}[2] = (6.567 \times 10^{-2})^3 \; 1.17 \times 10^{-9} = 3.31 \times 10^{-13}$$

at the end of 20 lines. This calculation is based on having a constant P_m which implies no RI buildup. It may, therefore, be considered worst case and as such means that the probability of getting a false sync during a sync interval is negligible.

Figure 21 is graphs of the probabilities of obtaining sync versus the line number for various input SNR, with and without the RI. This is simply the computational results from the above plotted for N = 3.

All calculable losses were included in arriving at the input SNR for these graphs. These losses are described in detail in paragraph 6.0, "Performance Limitation Factors". Perfect operation is also assumed, i.e., no frequency offset or time delay error effects were considered. The degradation due to frequency offset error is discussed in paragraph 6.2.

Figure 22 is a plot of P_s versus the idealized BER for 200 Kbps data transmitted in a 20 MHz bandwidth. Note that without the RI the sync processor performance can be considered marginal at a 10^{-2} data error probability but with the RI the P_s approaches unity. Also note that for this figure perfect (not ideal) performance is considered for the sync processor, while ideal (i.e., no degradation of any kind) performance is assumed for the video data recovery.

5.3.3.4 Sync Detection Logic Clock Stability. - As shown in Figure 20, the window generator and sync pulse generator have clock inputs. The stability requirements for the oscillator which provide these clocks depend on the stability required to maintain system synchronism during video processing. To accommodate small sync pulse timing errors the basic SDL clock operates at four times the chip rate, or 78.750 MHz. This frequency is divided by four to produce the 19.6875 MHz clocks for the mod 1250 window and sync pulse generators. When a reset pulse is applied through PG1 the lower ÷4 counter will be reset to its "00" state and the window counter reset to its "0000" state. By clocking the window counter from the second phase the ÷4 counter the next sync pulse will overlap the window 1250 counts later. Since the window width is four cycles of the 78.75 MHz clock, up to 25 nsec (plus or minus) of time error in the arrival of the sync pulse signal relative to the window can be compensated.

Once the sync sequence has been completed and the video portion of a field begins, the sync pulse generator continues to produce sync pulses at a 15.75 kHz rate, and any frequency error in the free running 78.75 MHz oscillator will result in a precession in the timing of the

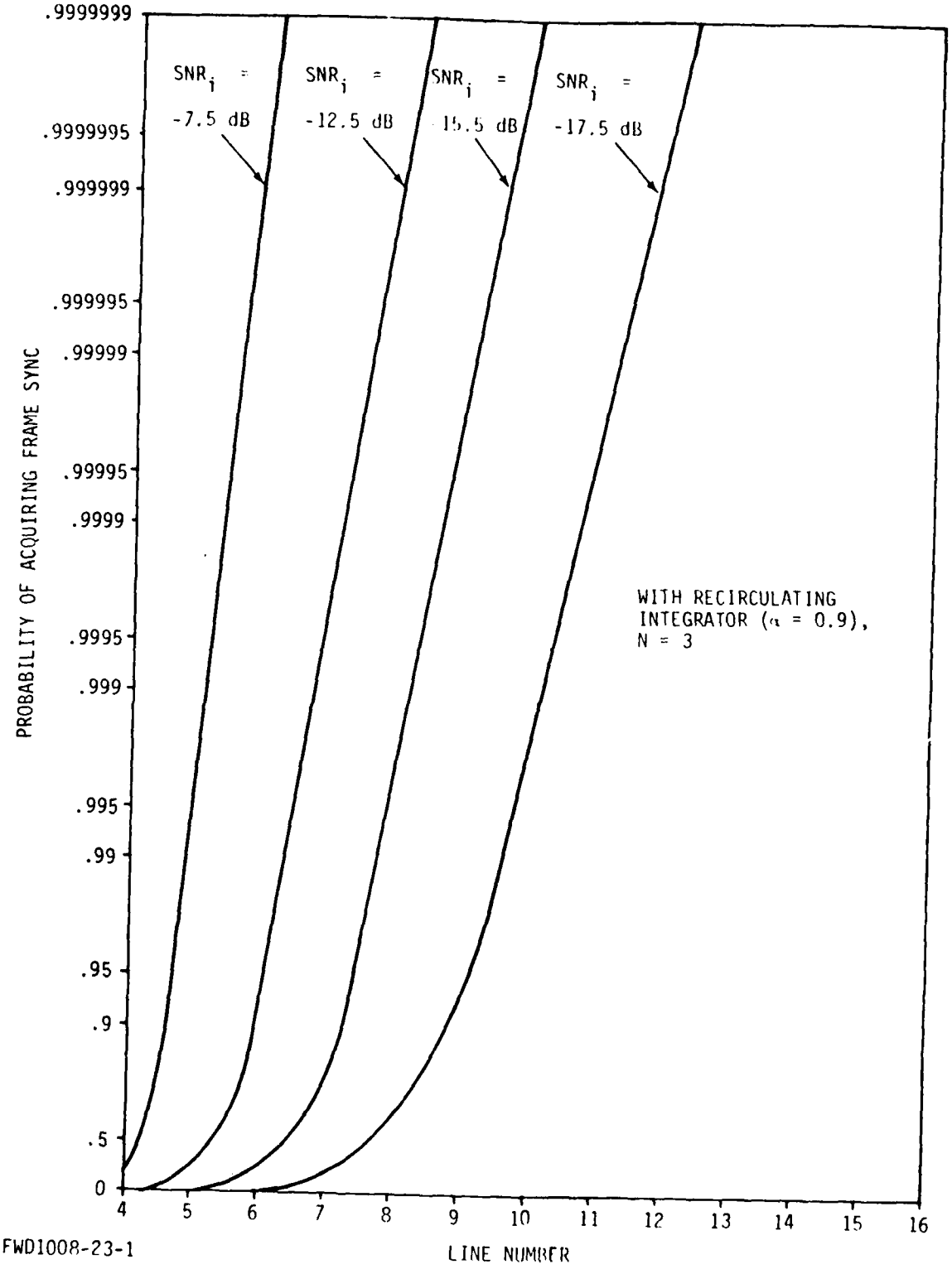
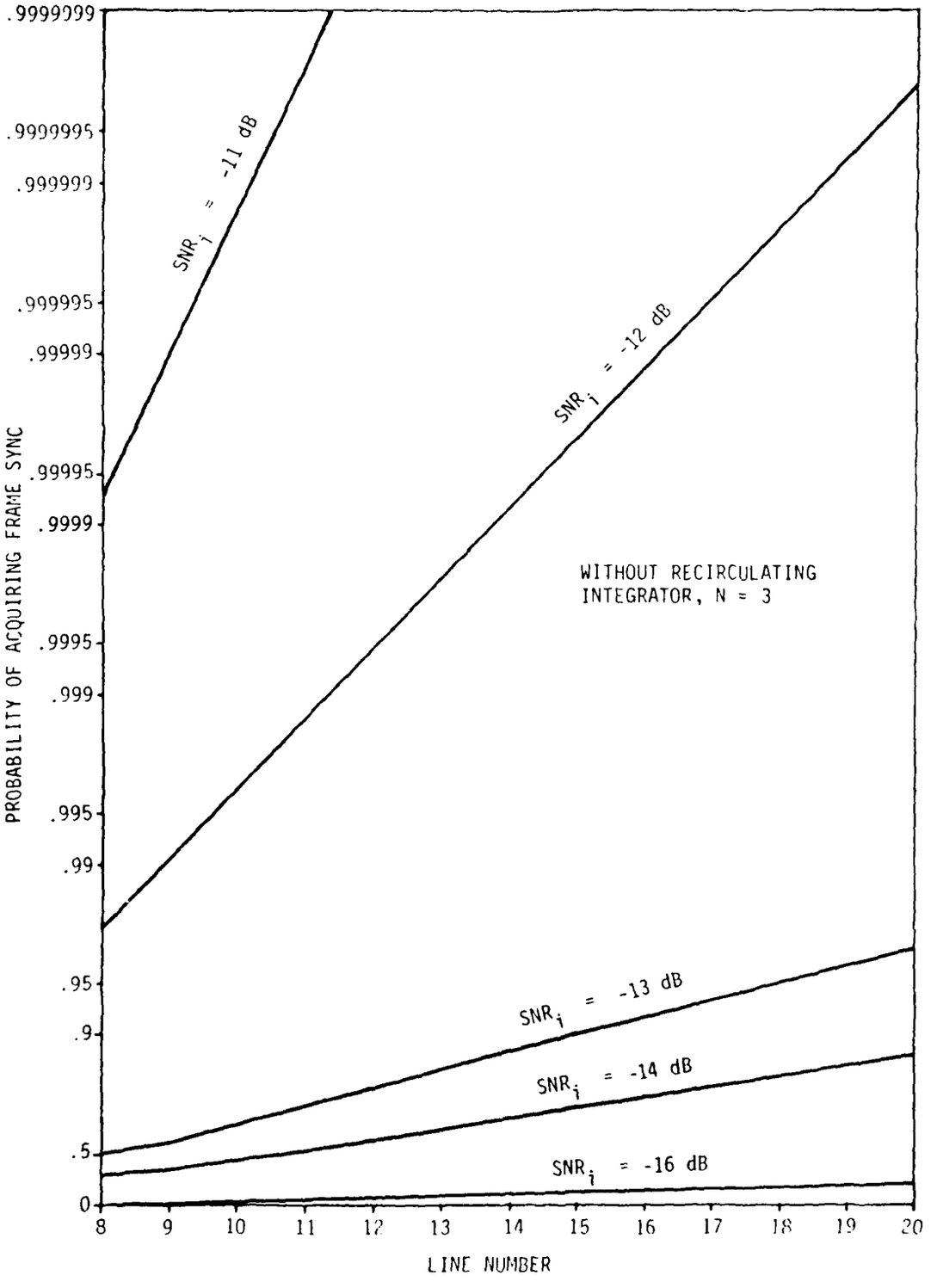
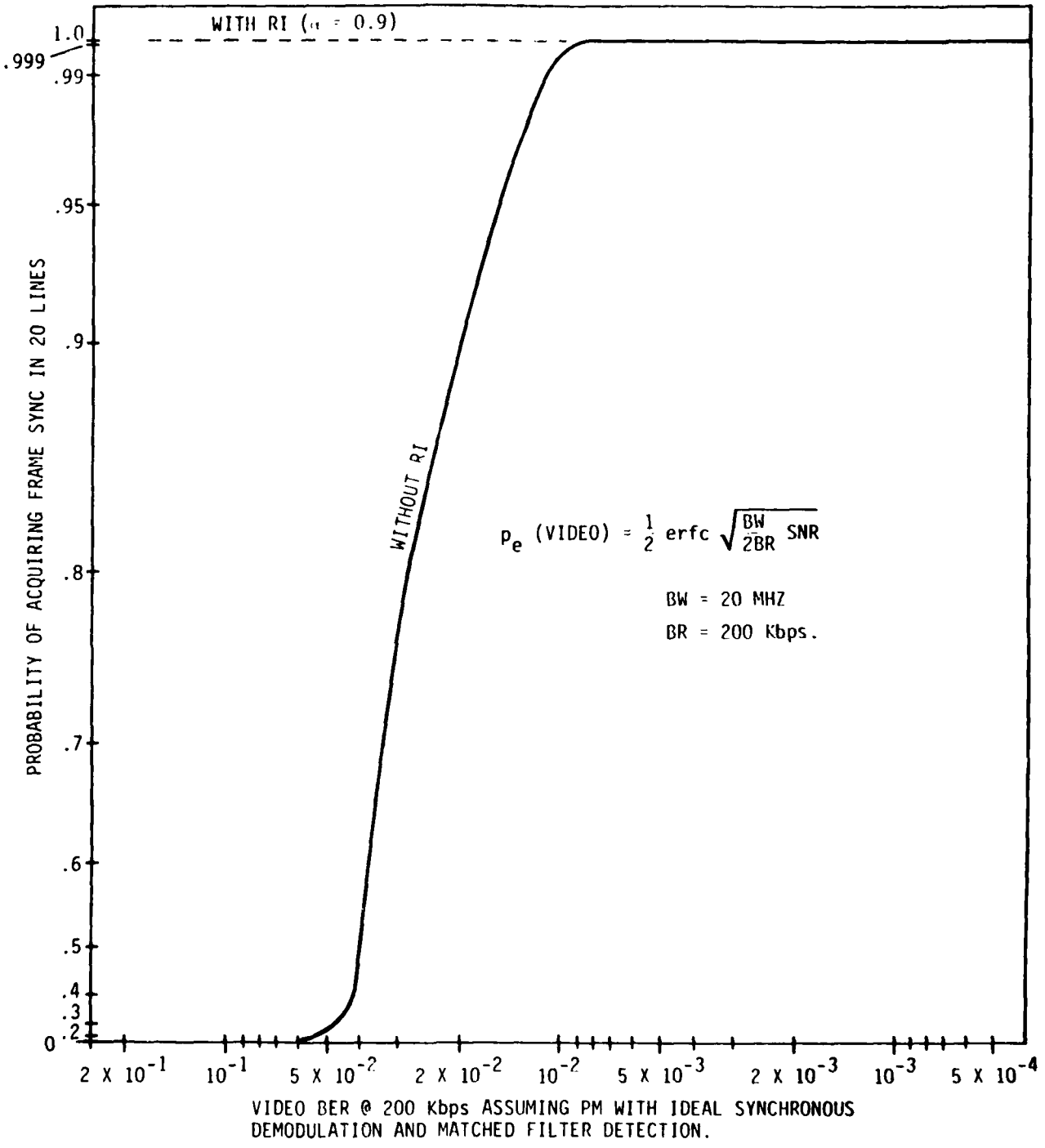


Figure 21. Probability of Acquiring Frame Sync Versus Line Number (Sheet 1 of 2).



FWD1008-23-2

Figure 21. Probability of Acquiring Frame Sync Versus Line Number (Sheet 2 of 2).



FWD1008-22

Figure 22. Calculated Probability of Acquiring Frame Sync at the end of 20 Lines Versus Corresponding Idealized Best Case Video Bit Error Rate

sync pulses provided to the video processor. The allowable sync pulse timing error that can be tolerated by the video processor depends to a certain extent upon the method chosen to spread spectrum modulate the video data. However, since the channel bandwidth is 20 MHz, a maximum sync pulse timing stability of within 50 nanoseconds can be inferred. Therefore, if it were desirable to hold sync pulse precession to within ±25 nanoseconds over a field interval (1/60 second), and oscillator stability, (long and short term), of about ±1.5 ppm is required. This level of stability is easily achieved with temperature compensated crystal oscillators.

6.0 PERFORMANCE LIMITATION FACTORS

The theoretical processing gain which is achievable by the system, as calculated in Paragraph 5.0, is based on the assumption of a non-band limited signal, perfect operation of the sub-sequence matched filters and recirculating integrator, and zero frequency offset at the link receiver IF output due to doppler or oscillator frequency error. In a practical system these conditions cannot be expected to occur, and therefore the factors which may affect these conditions in a practical system are of interest.

6.1 Band Limiting

The sync sequence signal generated by the RPV electronics has a $\frac{\sin X}{X}$ spectrum which theoretically occupies an infinite bandwidth. (Between the first nulls in the spectrum, the signal occupies 40 MHz of bandwidth, based upon the 20 MHz PN modulation rate.) In practice, the spectrum will be bandlimited by the RPV link transmitter to restrict the transmission channel-width requirements, reducing the achievable matched filter processing gain. The calculated processing gain loss for various system bandwidths is listed in Table 6-1.

Table 6-1. Processing Gain Loss Due to Bandlimiting

TRANSMISSION BANDWIDTH	LOSS IN PROCESSING GAIN
20 MHz	1.12 dB
25.4 MHz	0.71 dB
30 MHz	0.54 dB
40 MHz	0.44 dB
∞	0 dB

If the signal is restricted to a 20 MHz bandwidth, a processing gain loss of approximately 1.12 dB can be expected.

6.2 Temperature, Doppler and Frequency Offset Effects

6.2.1 Matched Filter. - The sensitivity of the matched filter processing gain to variations in temperature can be considered in terms of the fractional change in sub-sequence matched filter delay time with temperature. (This is true since the Recirculating Integrator delay line, which adds the outputs of the sub-sequence matched filters, is maintained at a constant temperature in an ovenized enclosure.)

As described by Bell*, the degradation in the peak response of a surface wave device PSK matched filter is given by $D = \frac{\sin(\pi N\phi)}{\pi N\phi}$, where ϕ = the fractional phase error of the device, and N = the number of carrier cycles integrated by the device. The fractional phase error for ST-Quartz as a function of temperature is given approximately by $\phi = -3.13 \times 10^{-8} \Delta T^2$, where ΔT is the deviation in substrate temperature from a reference temperature of 27.4 degrees centigrade. The sub-sequence matched filters each integrate 1456 cycles of carrier, which means a fractional phase error of about 60 ppm would be required for even a 0.1 dB degradation in sub-sequence matched filter array performance. This corresponds to a temperature variation of $\pm 44^{\circ}C$ which is considerably in excess of the expected temperature variation that the sync processor would experience in an operational environment.

Frequency offsets, on the other hand, whether due to link transmission equipment oscillator errors, or to doppler, must be considered in terms of the total length of the matched filter. Again, from Bell's* paper, the degradation of the matched filter output due to frequency offset is given by $D = \frac{\sin(\pi \Delta f T)}{\pi \Delta f T}$ where Δf = the frequency error in Hz and T = the total duration of the signal, in this case 63.492 μsecs. This equation predicts a complete null in matched filter output for a frequency offset of 15.75 kHz. For a degradation of 1 dB, the corresponding frequency offset is approximately 4.12 kHz.

If frequency offset due to oscillator instability is equally divided between the RPV and Ground Station, then the required stability at both locations for 4.12 kHz offset (1 dB degradation) at 4.5 GHz, 10 GHz and 15 GHz link transmission frequencies are as indicated in Table 6-2.

Table 6-2. Frequency Stability Required at Each Oscillator for 1 dB or Less Matched Filter Degradation Due to Frequency Offset

XMIT FREQ.	FREQ. STABILITY REQD.
4.5 GHz	0.47 PPM
10.0 GHz	0.21 PPM
15.0 GHz	0.14 PPM

However, doppler shift due to RPV-Ground Station relative velocity must also be considered. The amount of doppler shift at several values of RPV radial velocity are shown in Table 6-3.

---

*D.T. Bell, Jr., Phase Errors in Long Surface Wave Devices, 1972 IEEE Ultrasonics Symposium, Boston, Mass., October 1972, pp. 420-423.

Table 6-3. Frequency Offset Due to Doppler

XMIT FREQ.	RPV VELOCITY		
	100 KNOTS	200 KNOTS	300 KNOTS
4.5 GHz	772 Hz	1543 Hz	2316 Hz
10.0 GHz	1715 Hz	3430 Hz	5145 Hz
15.0 GHz	2572 Hz	5145 Hz	7716 Hz

If it is assumed that the RPV and Ground Station Oscillators can exhibit frequency stabilities of 0.1 ppm and that the RPV flies at a nominal velocity of 100 knots, then the maximum amount of processing gain degradation at the matched filter, as a function of transmit frequency, is shown in Table 6-4.

Table 6-4. Matched Filter
Degradation Due to Oscillator Error and Doppler

XMIT FREQ.	PROCESSING GAIN DEGRADATION
4.5 GHz	0.16 dB
10.0 GHz	0.8 dB
15.0 GHz	1.8 dB

6.2.2 Recirculating Integrator. - The processing gain provided by the Recirculating Integrator is significantly affected by oscillator offset in the RPV sync sequence generator clock oscillator, frequency offset introduced by the RPV transmit local oscillator, ground station receiver local oscillator, and by Recirculating Integrator loop delay error. For example, the degradation in Recirculating Integrator processing gain as a function of loop delay error is plotted in Figure 23 for a feedback factor, α, of 0.9, and twenty correlation pulses integrated. As can be seen, the processing gain is degraded 1 dB for a loop delay error of about 0.1 nanosec. If the loop delay error is identically zero, but the incoming signal frequency contains oscillator or doppler offset error, the same phenomenon occurs. For the case depicted in Figure 23, the amount of offset required for 1 dB degradation is approximately 220 Hz.

The Recirculating Integrator loop delay error is a function of the time delay temperature stability of the Recirculating Integrator

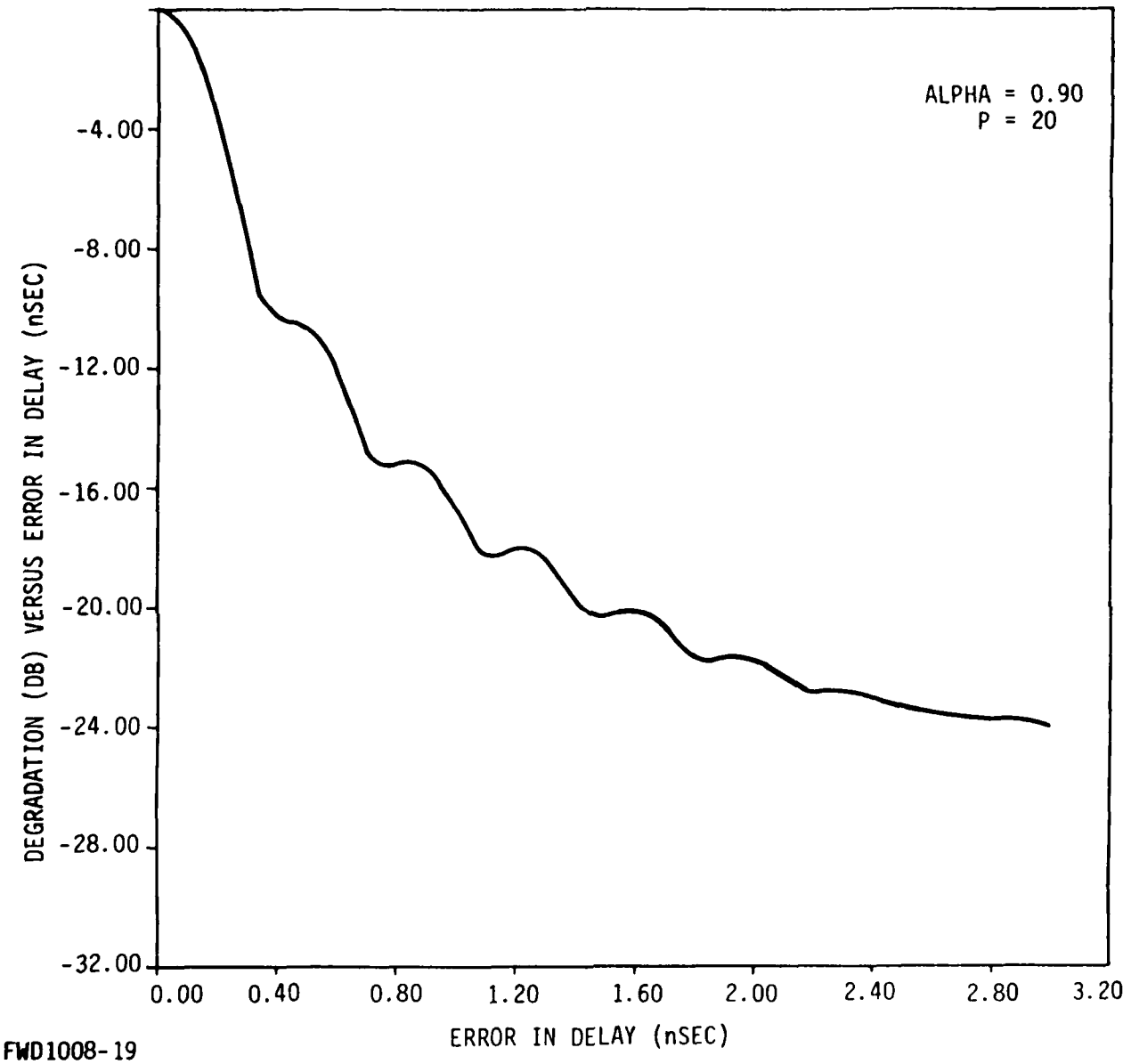


Figure 23. Degradation (dB) Versus Error in Delay (nSec)

Delay Line and this stability will be excellent using the oven stabilized RIDL enclosure described previously. Assuming that the Recirculating Integrator loop delay is stable, then the stability of the sync sequence repeat period is important. The stability of this period is determined by the stability of the 137.8125 MHz oscillator used as the clock reference in the RPV. The stability requirement on this oscillator is given by

$$\frac{\Delta f_{osc}}{f_{osc}} = \pm \frac{f_{osc} \Delta T_L}{(7)(1250) + f_{osc} \Delta T_L}$$

where Δf_{osc} is the allowable frequency error, f_{osc} is the oscillator frequency, and ΔT_L is the allowable error in sync sequence period length. For an oscillator frequency of 137.8125 MHz and a sequence period stability of 0.1 nanosecs, the required oscillator stability is ±1.6 ppm. Since it is possible to obtain temperature compensated crystal oscillators in this frequency range with ±0.5 ppm stability over a fairly broad temperature range (0^{o}C to 50^{o}C), the clock oscillator in the RPV should not be a significant problem if reasonable thermal control of the RPV electronics can be maintained.

The RPV transmit and ground station receiver local oscillator stabilities (and the doppler shift) are considerably more significant problems since the Recirculating Integrator processing gain is very sensitive to frequency offset. Note that it would appear at first glance that both doppler and transmit and receive oscillator offsets could be eliminated if the 137.8125 MHz PN-PSK signal generated in the RPV were impressed upon the down link carrier in the form of amplitude or frequency modulation, and then recovered at the ground station using an envelope detector or discriminator. In this case one would primarily be concerned with the frequency offset of the RPV clock oscillator and the equivalent doppler shift on the 137.8125 MHz PN-PSK carrier, which is insignificant. However, both of these forms of modulation exhibit a sharp signal to noise ratio threshold effect which would significantly reduce the equivalent signal to noise ratio at the sync processor input when the signal was received at low (or negative) signal to noise ratios.

An alternative means of dealing with the effects of frequency offset on the RI is to modify the feedback factor, α. The net processing gain of the RI is given by the expression

$$G_p(\alpha, L, \phi) = 10 \log \left[\frac{(1-\alpha^2)(\alpha^{2L} - 2\alpha^{L} \cos L\phi + 1)}{\alpha^2 - 2\alpha \cos\phi + 1} \right]$$

where α is the feedback factor ($0<\alpha<1$), L the line number ($1 \leq L \leq 20$) in this case), and ϕ is the fractional phase error defined by

$$\phi = 2\pi(f\Delta T + T\Delta f) \text{ radians}$$

where f is the carrier frequency, Δf is the frequency error, T is the RI delay (63.492 μsec in this case), and ΔT the delay error.

Rewriting the above expression,

$$G_p(\alpha,L,\phi) = 10 \log (1-\alpha^2) + 10 \log (\alpha^{2L} - 2\alpha^L \cos L\phi + 1) - 10 \log (\alpha^2 - 2\alpha \cos \phi + 1),$$

produces an expression in which L appears in only one term. The effects of neglecting this term can be considered for L = 20.

Let ϵ_G be the maximum allowable error in G_p due to neglecting the center term:

$$10 \log (\alpha^{40} - 2\alpha^{20} \cos 20\phi + 1) \leq \epsilon_G, \quad L = 20$$

$$\alpha^{40} - 2\alpha^{20} \cos 20\phi + 1 \leq 10^{\frac{\epsilon_G}{10}}$$

This quantity will be maximum for $\cos 20\phi = -1$ so with this worst case condition:

$$\alpha^{40} + 2\alpha^{20} + 1 - 10^{\frac{\epsilon_G}{10}} \leq 0$$

$$\alpha \leq \left[10^{\frac{\epsilon_G}{20}} - 1 \right]^{1/20}$$

is an expression for the maximum value of α for a given error in RI processing gain at the end of 20 lines.

Alternatively, a criteria for α is that

$$20 \log (\alpha^{20} + 1) \leq \epsilon_G.$$

After neglecting the middle term of the original expression for G_p the remainder which is a function of α and φ can be maximized with respect to α for a given φ (and, so, a given frequency error) to yield the optimum α:

$$\frac{dG_p}{d\alpha} \approx \frac{d}{d\alpha} \left(\frac{1-\alpha^2}{\alpha^2 - 2\alpha \cos\phi + 1} \right) = 0$$

$$\therefore \alpha_{opt}(\phi) = \frac{1 \pm \sin\phi}{\cos\phi} = \pm \left(\frac{1 - \sin\phi}{1 + \sin\phi} \right)^{1/2}$$

Substituting this quantity into the original approxmiate expression for G_p gives $G_{pmax}(\phi)$;

$$G_{pmax}(\phi) \approx 10 \log \left[\frac{1 - \frac{1-\sin\phi}{1+\sin\phi}}{\frac{1-\sin\phi}{1+\sin\phi} - 2\left(\frac{1+\sin\phi}{\cos\phi}\right)\cos\phi + 1} \right] = 10 \log (\csc\phi).$$

Therefore, given a ϕ as determined above, the approximate maximum obtainable RI processing gain can be determined. The corresponding optimum α can be found using the expression for $\alpha_{opt}(\phi)$. The error, in dB, of the processing gain due to the original approximation can then be determined from the equation for ε_G.

Some examples of these calculations are given in Table 6-5. Values for ϕ are chosen based upon the data in Table 6-2 for 100 knots RPV velocity and assumming 0.1 ppm frequency source accuracy in the RPV and 0.01 ppm frequency source accuracy at the ground station.

Table 6-5. RI Processing Gain With Frequency Error

VIDEO LINK OPERATING FREQ.	FREQ. ERROR[1]	ϕ	MAX. G_p	at α =	$\varepsilon_p \leq$
4.5 GHz	772 Hz[2]	17.6°	5.18 dB	.73	.02 dB
4.5 GHz	1267 Hz	29°	3.15 dB	.59	2.2×10^{-4} dB
10.0 GHz	2815 Hz	64.3°	0.45 dB	.23	0 dB
15.0 GHz	4222 Hz	96.5°	0.03 dB	-.06	0 dB

[1]Frequency error is the sum: $(0.1 + 0.01) \times 10^{-6}$ x operating frequency + doppler shift.

[2]Doppler shift only.

The above data indicates that the use of a Recirculating Integrator to obtain additional processing gain will not be practical without some provision for dealing with frequency offset of the RI carrier. This problem has been considered and two possible solutions have emerged.

One is to track out the offset by the use of a phase locked loop in which a locally generated PN sequence is cross correlated with the received PN sequence. The correlation pulses from the PN matched filters (which are not degraded significantly due to frequency offset - see

Table 6-1) would be used to preset the local PN generator which then is made to track the incoming sequence and maximize the cross correlation peak. After only a few (e.g., 3 or 4) lines the frequency offset could be corrected sufficiently to produce up to a 10 dB processing gain in the RI for the remaining lines.

The second technique, which could be used in conjunction with the first, is to envelope detect the output of the PN matched filter and remodulate the resulting pulses onto the RI using a highly stable local oscillator. Following the envelope detector and prior to the remodulator, nonlinear signal processing would be employed to enhance the SNR of the received sync pulses. This nonlinear processing appears to provide sufficient effective signal enhancement to more than overcome the losses in SNR due to envelope detection, however, a definite threshold effect is also anticipated. Because the RI carrier could be very well controlled in frequency, a net processing gain of 10 dB in the RI appears feasible with this approach.

Detailed analysis of either of the above two solutions is beyond the scope of this study due to the significant impact to the sync processor design. Additional investigation to examine both techniques in detail is suggested since the frequency offset problem is so significant in terms of overall system performance.

7.0 RESULTS AND CONCLUSIONS

From Figures 21 and 22 it is evident that without the Recirculating Integrator the Sync Processor performance will be marginal; however, with the RI and its added processing gain, performance is very good even below -17 dB input SNR. In fact, considering Figure 21 (sheet 1), there appears to be a generous safety margin in the probability of obtaining sync with the RI included.

This performance is contingent, however, on the processing gain contribution of the RI which is in turn a sensitive function of time delay and frequency offset error. As discussed in paragraph 5.3.2, the time delay error can be maintained well within the required limits. Frequency offset error, on the other hand, is determined by oscillator and frequency source inaccuracies and instabilities, and by doppler shift in the received signal spectrum. Table 6-5 gives the maximum RI processing gain as a function of frequency error assuming excellent frequency stability and accuracy in the microwave sources used. From Table 6-5, at a 10 GHz operating frequency, the maximum calculated RI processing gain is seen to be only 0.45 dB, which certainly would not justify the expense of the RI.

Two solutions were proposed to deal with the frequency error problems. Application of these solutions, which are briefly discussed at the end of paragraph 6.0, would only add to the value of the work presented here. Further benefits may also be derived from incorporating the proposed solutions. Both a phase-coherent clock and a start-of-video identification pulse could be derived during the frame sync interval. This additional capability would provide information of significant value in optimum demodulation and detection of the spread-spectrum video transmission signal and, therefore, enhance the overall system performance.

FOURIER TRANSFORMATION OF TELEVISION SIGNALS BY NONLINEAR DELAY LINE TECHNIQUES

T. M. Reeder
United Aircraft Research Laboratories

N921957-F

FOURIER TRANSFORMATION OF TELEVISION SIGNALS BY NONLINEAR DELAY LINE TECHNIQUES

FINAL TECHNICAL REPORT ON
CONTRACT N66001-74-C-0497

Prepared for

NAVAL UNDERSEA CENTER
SAN DIEGO, CA. 92132

by

T.M. Reeder

March 1975

United Aircraft
Research Laboratories
UNITED AIRCRAFT CORPORATION
EAST HARTFORD, CONNECTICUT 06108

N921957-F

Fourier Transformation of Television Signals by Nonlinear Delay Line Techniques

TABLE OF CONTENTS

ABSTRACT

This report describes an initial research and development program on a new Surface Acoustic Wave (SAW) module which is capable of performing the Discrete Fourier Transform (DFT) of a P sample video waveform in real time. The new DFT module is based on a programmable version of the earlier reported Diode-Convolver nonlinear delay line device. A theory of the Programmable Diode-Convolver is given which provides a complete first order description of the device in terms of output versus diode bias level, dynamic range, and maximum Fourier bandwidth. Experiments with a 12 tap, discrete diode PDC DFT module exhibited a tap dynamic range of more than 40 dB. Experiments with a 32 tap unit using silicon-on-sapphire diodes demonstrated a Fourier bandwidth which was electronically adjustable from zero to beyond 10 MHz.

ACKNOWLEDGMENTS

The author is pleased to acknowledge the many individuals who made important contributions during the course of this program. H. J. Whitehouse and J. M. Speiser of NUC provided the mathematical insight and useful system description that led to the application of the Diode-Convolver as a DFT module. A number of discussions with H. J. Whitehouse, J. M. Speiser and W. D. Squire were very helpful in carrying out the present program. UAC Research Laboratories personnel who made significant contributions were A. J. DeMaria and M. Gilden who provided program management, E. Branciforte who fabricated the experimental PDC modules, S. Sheades and R. Rukus who carried out experimental measurements, and T. Grudkowski who performed the detailed tap output measurements reported for the 12 tap module.

LIST OF ILLUSTRATIONS

N921957-F

Fourier Transformation of Television Signals By Nonlinear Delay Line Techniques

I. INTRODUCTION

A. Program Scope

This report describes an initial research and development program on a new Surface Acoustic Wave (SAW) module which is capable of performing the Discrete Fourier Transform (DFT) of a P sample video signal waveform in real time. The new DFT module is based on a programmable version of the UARL Diode-Convolver device (Refs. 1-4). The parallel input-serial output configuration of the Programmable Diode-Convolver (PDC) provides a unique example of the general class of DFT devices first proposed by H. J. Whitehouse and coworkers at NUC (Refs. 5-7). Our major goal in the present program was to demonstrate that the PDC is capable of implementing the NUC transform configuration with large bandwidth ($B \geq 10$ MHz). A wide bandwidth module will be immediately useful in advanced television communication links and will provide a signal processing capability not likely to be achieved by competitive approaches using digital computers (Refs. 8-9) or Charge Coupled Device (CCD) processors (Ref. 10).

The scope of this program was to perform an initial investigation of the feasibility, governing parameters, and limitations for the use of the PDC device as a real time DFT module. Theoretical analysis was carried out to develop a PDC design model that relates the component acoustic and electric parameters to the DFT output versus tap bias, dynamic range, and maximum Fourier bandwidth. Diagnostic experiments were performed using PDC modules with the following characteristics:

12 and 32 tap parallel input

Fourier bandwidth up to 20 MHz

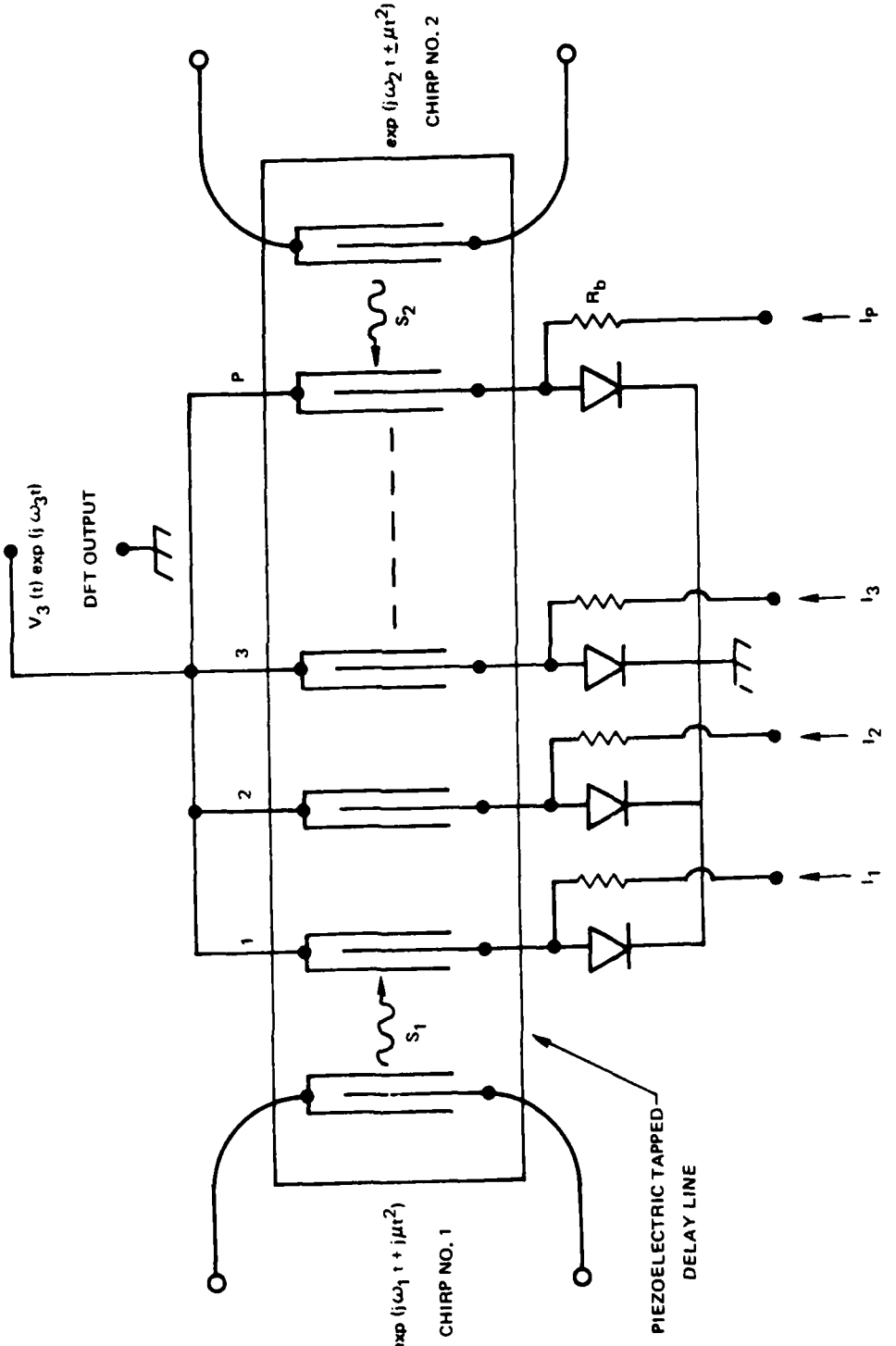
Reference chirp signal inputs centered at approximately 120 and 180 MHz

DFT output centered at 60 MHz

The experimental PDC modules were built under a concurrent UARL in-house program whose goal was to investigate the fabrication of advanced PDC modules using state-of-the-art integrated circuit and SAW delay line technology. These experimental devices were made available to the present program at no charge.

FIG. 1-1

PROGRAMMABLE DIODE-CONVOLVER DFT MODULE



N10-282-4

B. Operation of the PDC as a DFT Module

As is shown schematically in Fig. I-1, the Programmable Diode-Convolver is a hybrid microelectric device which consists of a piezoelectric tapped delay line and an attached semiconductor diode array. The PDC is a unique example of a general class of nonlinear delay line devices (Ref. 11) which perform the real time convolution of two input signals by use of nonlinear mixing in a delay line interaction region of time length T. If rf signals of the form $V_1(t)\exp(j\omega_1 t)$ are applied to the transducers at Ports 1 and 2 of the delay line, the convolution output is the complex waveform $V_3(t)$ received at Port 3 with carrier frequency equal to the sum or difference of input frequencies ω_1 and ω_3. Under the conditions developed in Section II, it is convenient to operate the PDC with difference frequency output. The output waveform then has the serial product form

$$V_3(t) = A\sum_{p=1}^{P} g_p\, V_1\,(t-p\Delta T)\, V_2^{*}\,(t+p\Delta T) \qquad \text{(I-1)}$$

where P is the number of delay line taps, $\Delta T = T/P$ is the acoustic transit time between taps, g_p is tap weighting amplitude controlled by the diode bias current, and A is a constant. Programmable operation of the PDC is derived from the fact that the coefficients g_p can be selected individually from a P output programmable current supply.

The PDC becomes a DFT processor when chirp signals with bandwidth $B = \mu T/\pi$ and form $\exp(j\omega_i t + j\mu t^2)$ are applied to Ports 1 and 2 in Fig. I-1. In this case the waveform seen at Port 3 can be from Eq. (I-1),

$$V_3(t) = A\sum_{p=1}^{P} g_p e^{-j4\mu p\Delta T t} \quad . \qquad \text{(I-2)}$$

At time $t = m/2B = m\pi/2\mu\Delta TP$ this becomes

$$V_3(t) = A\sum_{p=1}^{P} g_p e^{-j2\pi mp/P} \qquad \text{(I-3)}$$

which, within a constant, is equal to the usual definition of the DFT over the tap coefficients g_p.

C. Method of Approach

The method of approach used in this program was to analyze the operation of the Diode-Convolver DFT module in terms of Eq. (I-3). Previous work on the Diode-Convolver had considered only the applications where the diode-taps are equally biased in series or parallel. Thus, this was the first program to analyze the device as a PDC where the diode currents could be individually selected or programmed. The earlier theory was extended here to describe operation with programmable taps and the operation of the PDC as a DFT device was considered in terms of tap output versus bias level, dynamic range, and maximum Fourier bandwidth. With this theory as a guide, experiments were carried out on 12 and 32 tap PDC devices to verify the expected characteristics and to find limitations in the present fabrication technology. The theory predictions of Section II were substantially verified by the experiments described in Section III. The advantages and limitations of the Diode-Convolver DFT module were clearly delineated during this program. Section IV presents our conclusions and recommendations for the future logically development of this interesting, new device.

II. APPLICATION OF THE PROGRAMMABLE DIODE-CONVOLVER AS A REAL TIME DFT MODULE

A. Introduction

The basic characteristics of Diode-Convolver devices have been investigated on earlier programs directed toward electronically variable radar correlation applications (Ref. 4). The theory and experiment for these radar correlators considered only the case where all diode-taps were biased equally in parallel. Strictly speaking, these devices were not programmable; the amplitude of individual taps could not be adjusted by programming the diode currents. In this section we review the basic theory of Diode-Convolvers, describe the operation of the PDC as a DFT module, and relate the operating characteristics of the DFT module to the PDC parameters.

B. Principles of Operation

The signal processing capability of the Diode-Convolver is based on the parametric interaction of modulated acoustic waves in a discretely tapped, nonlinear interaction region. As shown schematically in Fig. II-1, the interaction region in the Diode-Convolver consists of an array of SAW delay line taps which are connected to forward biased semiconductor diodes. Modulated voltages applied to Ports 1 and 2 of the device give rise to SAW strain waves (S_1 and S_2) which travel into the interaction region. In turn, these waves excite voltages at individual taps which cause currents to flow in the diodes at input frequencies f_1 and f_2. Due to the diode nonlinearity, currents and voltages are also excited in each diode-tap at the sum and difference frequency, $f_1 \pm f_2$, which are summed at the common output, Port 3.

The basic features of this nonlinear interaction may be derived by considering the nonlinear interaction at a single tap. Suppose that voltages of the form $V_i(t)$ $\exp(j\omega_i t)$ are applied to transducers at Ports 1 and 2 of the SAW delay line. The functions $V_i(t)$ are the voltage waveforms or complex envelops representing input signal modulation while $f_i = \omega_i/2\pi$ are the input carrier frequencies. Traveling strain waves will be excited inside the delay line interaction region with the form

$$S_1(t,z) = S_1(t_-) \quad \exp\ (j\omega_1 t_-) \tag{II-1}$$

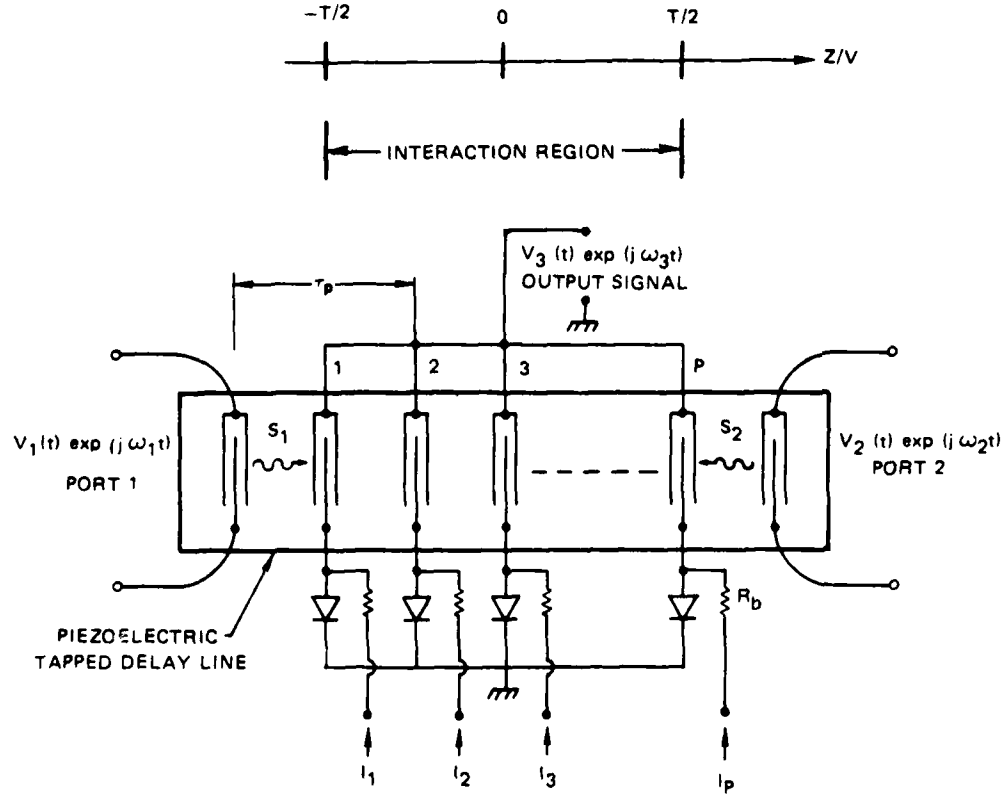
$$S_2(t,z) = S_2(t_+) \quad \exp\ (j\omega_2 t_+) \tag{II-2}$$

where t_- and t_+ are the traveling wave time coordinates

$$t_- = t - z/v \tag{II-3}$$

FIG. II-1

THE PROGRAMMABLE DIODE-CONVOLVER (PDC)



$$t_+ = t + z/v \qquad \text{II-4}$$

while v is the wave velocity and z is the delay line coordinate. Since the taps are equi-spaced with transit time $\Delta T = \Delta L/v$ between taps, it is convenient to write the tap position z_p in time units. Assuming that the total tap count P is an even number, the tap position becomes

$$t_p = z_p/v = (\Delta T/2)(2p - P + 1). \qquad \text{II-5}$$

Since the delay line input transducers and interaction region taps may be assumed to be linear for the signal levels used in the Diode-Convolver, the voltage excited at the pth tap due to strain waves excited by voltages applied to Ports 1 and 2 will have the form

$$V_{pi}(t)\exp(j\omega_i t) = A_{pi}\ V_i(t)\ \exp(j\omega_i t \pm j\omega_i t_p) \qquad \text{II-6}$$

where A_{pi} is a frequency dependent constant determined by the input transducer and interaction tap transfer functions.

With the above discussion as a background, we are now ready to evaluate the nonlinear output generated at Port 3 due to wave interaction at the pth tap. Our basic assumptions are that if voltages V_{p1} and V_{p2} are excited due to input signals with carrier frequency f_1 and f_2:

1) the nonlinear diode-tap responds with a voltage and current whose waveform is proportional to the product of the two input voltage waveforms and whose frequency is either the sum or difference of the input carrier frequencies, and

2) the nonlinear signals excited at each tap are weakly coupled to the delay line so that the total nonlinear output at Port 3 in Fig. II-1 is simply the sum of nonlinear signals excited at all taps.

Under these assumptions, the voltage generated at Port 3 in Fig. II-1 due to nonlinear interaction at the pth tap reduces to a simple form when the output is filtered to receive only the sum or difference output. For example, if we chose to receive only the difference frequency output,

$$V_{p3}(t)\ \exp(j\omega_3 t) = g_p\ V_1(t-t_p)\ V_2^*(t+t_p)\ \exp\left[j(\omega_2-\omega_1)t\right]\ \exp\left[j(\omega_1+\omega_2)t_p\right], \qquad \text{II-7}$$

where g_p is a combined proportionality constant representing the transducer-tap transfer functions and diode nonlinear coupling coefficient. The development of Eq. (II-7) is discussed more fully in Ref. 4.

The usefulness of the Diode-Convolver as a convolution device is realized by noting that the phase term $\exp\left[j(\omega_1+\omega_2)t_p\right]$ in Eq. (II-7) can be simplified to

$$\exp\left[j(\omega_1 + \omega_2)t_p\right] = \exp\left[j\theta_0 + j2\pi np\right] \qquad \text{(II-8)}$$

where θ_0 is a constant and np is an integer. This simplification occurs when

$$f_1 + f_2 = n/\Delta T \qquad \text{(II-9)}$$

where n is an integer and ΔT is the inter-tap transit time defined earlier. Equation (II-9) together with the frequency mixing (hetrodyne) equation,

$$f_2 - f_1 = f_3 \ , \qquad \text{(II-10)}$$

define the input carrier frequencies in terms of the tap spacing and the desired Port 3 carrier frequency. These two equations define the nonlinear parametric operating conditions (Ref. 11).

Under the above conditions phase term $\exp j(\omega_1+\omega_2)t_p$ reduces to a complex constant. The <u>total</u> difference frequency output received at Port 3 can then be written

$$V_3(t) = A \sum_{P=1}^{P} g_p \, V_1(t-t_p) \, V_2^* \, (t+t_p) \qquad \text{(II-11)}$$

where $A = \exp(j\theta_0)$. Equation (II-11) is recognized as the serial product convolution of modulation waveform V_1 with the conjugate of waveform V_2.

C. Application of the PDC as a DFT Module

The application of the PDC as a DFT device comes from the observation that a convolution device can be used in Fourier transform operations by performing the following three step signal processing procedure: 1) multiply the signal to be transformed by a chirp signal, 2) convolve the result of step 1) with a second chirp, and 3) post multiply the result by a third chirp. This technique has been used for many years in optical Fourier transforms (Ref. 12) and more recently has been applied to the computation of Discrete Fourier Transforms by use of the chirp-Z algorithm (Ref. 13). In a series of detailed theoretical and experimental programs dedicated to finding ways to economically transmit wide bandwidth television signals over moderate bandwidth, highly secure transmission channels, workers at NUC proposed and demonstrated that the chirp-Z approach to DFT computations could be implemented in delay line technologies using SAW and CCD devices (Refs. 5, 6, 7, 14, 15). Compared to the well known transform computation capability of digital computer processors, the delay line approach has advantages in: 1) wide bandwidth operation, 2) small size, weight, power consumption, and 3) relatively simple, planar fabrication. The powerful advantages of the Fourier transform in reducing television signal redundancy without significantly sacrificing picture detail have been well proven by research programs using digital computers at slower than real time rates (Refs. 8, 9, 16, 17). The NUC approach using delay line technology promises to provide the advantages of the Fourier transform method in a form that is capable of large bandwidth (10 to 100 MHz) and can perform at real time transmission rates.

In operation as a DFT processor, the PDC performs the three operations of the Chirp-Z transform in a single nonlinear delay line interaction region of time length T. Suppose that chirp signals with bandwidth $B = \mu T/\pi$ and form $\exp(j\omega_i + j\mu t^2)$ are applied to Ports 1 and 2 in Fig. II-1. Assuming that the carrier frequency parametric relations [Eqs. (II-9, -10)] are satisfied, we can substitute these chirp signal expressions directly into Eq. (II- 7) and rearrange terms to show that Eq. (II-11) becomes

$$V_3(t) = A\sum_{p=1}^{P} g_p \, e^{-j4\mu t t_p} \quad . \tag{II-12}$$

If we express t_p in terms of tap number p given by Eq. (II-5) and renumber the taps so that p becomes p-1, Eq. (II-12) becomes

$$V_3(t) = A'\sum_{p=0}^{P-1} g_p \, e^{-j4\mu t \Delta T p} \tag{II-13}$$

where $A' = A \exp[j2\pi\mu\Delta T(P + 1)t]$ is a complex multiplier that does not vary with p. Since $\mu = \pi B/T$ and $\Delta T = T/P$, we can show that at time $t = m/2B$

$$V_3(t) = A' \sum_{p=0}^{P-1} g_p \, e^{-j2\pi mp/P} \quad . \qquad \text{(II-14)}$$

The summation in Eq. (II-14) is equivalent to the usual definition of the DFT, and the quantity A' has the form of a complex sinusoid of frequency B(P + 1)/P. We conclude that the Port 3 modulation output of the PDC when driven by chirp signal is simply the DFT of tap weights g_p taken over bandwidth B and multiplied by sinusoid A'.

The above analysis has shown that the PDC device can be utilized in a relatively simple DFT circuit. It will be instructive to consider examples illustrating the use of the PDC in DFT operations. Since input chirp signals are required at Ports 1 and 2, we shall define the PDC DFT module as a complete unit that provides all required chirp signal and associated circuits such that a P line input and timing signal are all that is required to produce the standard DFT output represented by the summation in Eq. (II-14).

Figure II-2 shows the most direct way of using the PDC DFT module. With a general time varying input, $g_p(t)$. the input signal is applied to a demultiplexer which sequentially switches $g_p^p(t)$ to sample and hold (S/H) circuits connected to each PDC tap. The clock circuit provides timing for the demultiplexer-S/H circuit and also for the PDC chirp inputs. As we shall see later in this section, PDC units can already be built with Fourier bandwidths over 10 MHz and tap counts of 32 or more on 37 ns spacing. However, input demultiplexer-S/H circuits to match this capability are not yet available in a form commensurate with the PDC size (i.e., approximately 0.005 inch tap spacing).

Figure II-3 shows a more general DFT circuit based on the two dimensional DFT approach proposed at NUC (Ref. 6). Here, the input demultiplexer drives P identical transform devices of length N which in turn drive the P taps of the PDC module. The functions $S_1(t)$ through $S_{P-1}(t)$ are complex phasors which are used to subtract out unwanted phase terms in the first stage transform devices. The advantage of the circuit in Fig. II-3 is that the first stage devices do not require large bandwidth since they are fed samples at a rate that is 1/P times the input data rate. However, these devices must have long signal processing length since they will be required to process at least one data block ($\sim 50\,\mu s$ at a time. The output DFT module, on the other hand, will not require long signal processing time since it will recycle in a time 1/N times the input message length ($\sim 50\,\mu s$). However, the output module must provide a maximum Fourier bandwidth commensurate with the input data rate.

The circuit in Fig. II-3 appears to be well suited to a combination of CCD and SAW technologies. The first stage transform devices can be implemented in CCD technology for bandwidths up to 5 MHz and signal processing lengths from 50 to several hundred μs (Ref. 10). Signal processing lengths over 20 μs are difficult for SAW devices. On the other hand, operation with bandwidth greater than 5 MHz is very difficult for CCD devices. Thus, the wide bandwidth, simple configuration of the PDC DFT module is likely to remain significantly ahead of CCD technology for applications as a wide bandwidth, moderate signal processing length ($< 10\,\mu s$) DFT device.

HIGH SPEED DFT SUBSYSTEM USING THE PDC SAW DEVICE DFT MODULE

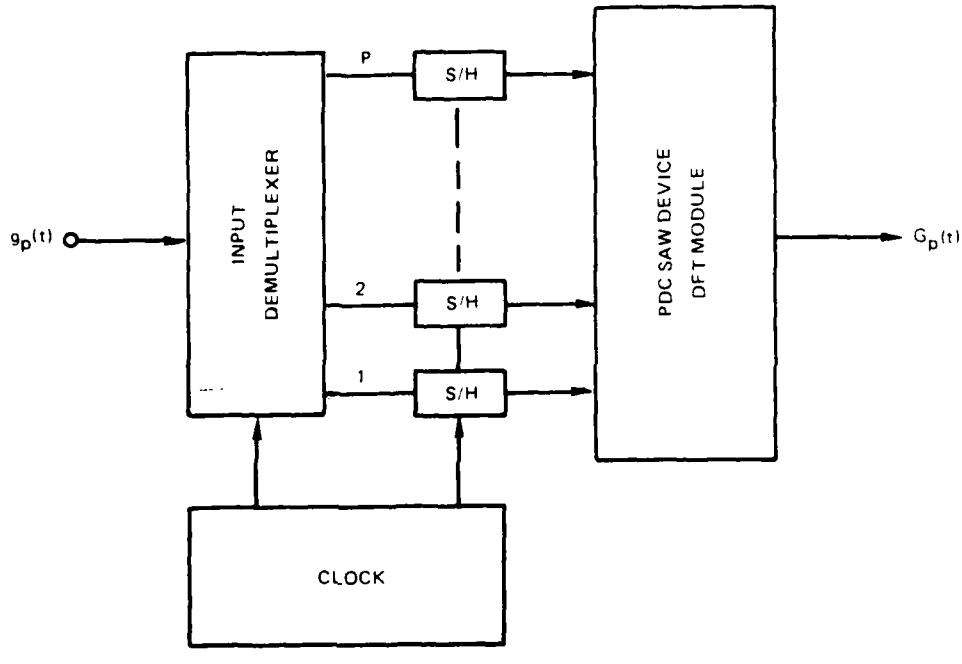
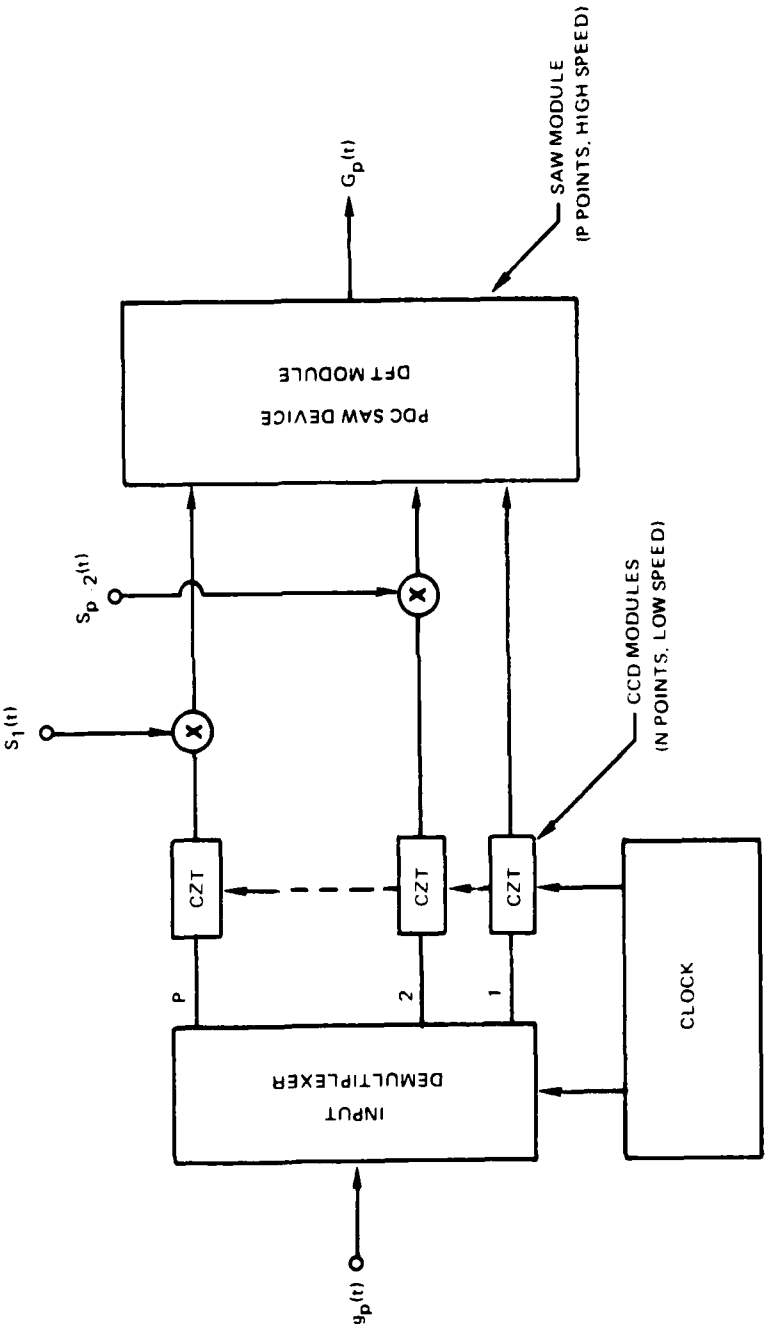


FIG. II-3

HIGH RESOLUTION DFT SUBSYSTEM USING BOTH CCD AND SAW TECHNOLOGIES



D. Analysis of DFT Module Operation in Terms of PDC Parameters

Detailed analysis of the PDC DFT module is most easily carried out using an equivalent circuit model to represent the acousto-electric and nonlinear transfer function response of the PDC device. In order to clearly delineate the effects of the PDC tapped interaction region and to keep the analysis from becoming unnecessarily complicated, we shall make the following assumptions: 1) the PDC Port 1 and 2 transducers and the interaction region transducers-taps have bandwidth much larger than the operating Fourier bandwidth and 2) the interaction region taps have zero acoustic length. The essential features of the PDC can then be described with the equivalent circuits shown in Fig. II-4. The circuit is Fig. II-4a may be related to the PDC schematic in Fig. II-1 as follows. The SAW transducer-tap is modelled by a series circuit consisting of a radiation resistance R_a, tap capacitance C_T, and two voltage generators that correspond to tap excitation at carrier frequencies f_1 and f_2. The tap circuit is in series with the pth tap diode which is connected in parallel with the impedance $Z_p/(P-1)$ due to the other P-1 diode-taps and the Port 3 output load resistance R_L.

Analysis of the diode-tap nonlinear coupling is more easily carried out by use of the equivalent parallel circuit shown in Fig. II-4b. Here, the generator admittance is

$$Y_{gi} = \left[R_{ai} + \frac{1}{j\omega_i C_T} + \frac{1}{(P-1)/Z_{pi} + 1/R_L} \right]^{-1}, \qquad \text{(II-15)}$$

and the current generators are $I_{gi} = V_{gi}\, Y_{gi}$. The subscript i corresponds to evaluation at frequency $f_i = \omega_i/2\pi$. Since the diode is in forward bias, we assume that its admittance is real and can be represented by expanding the nonlinear conductance in a power series

$$G(V_p) = \sum_{n=o}^{\infty} G_n V_p^n. \qquad \text{(II-16)}$$

By considering first the small signal solution, we may assume that the power series is adequately approximated by the first two terms.

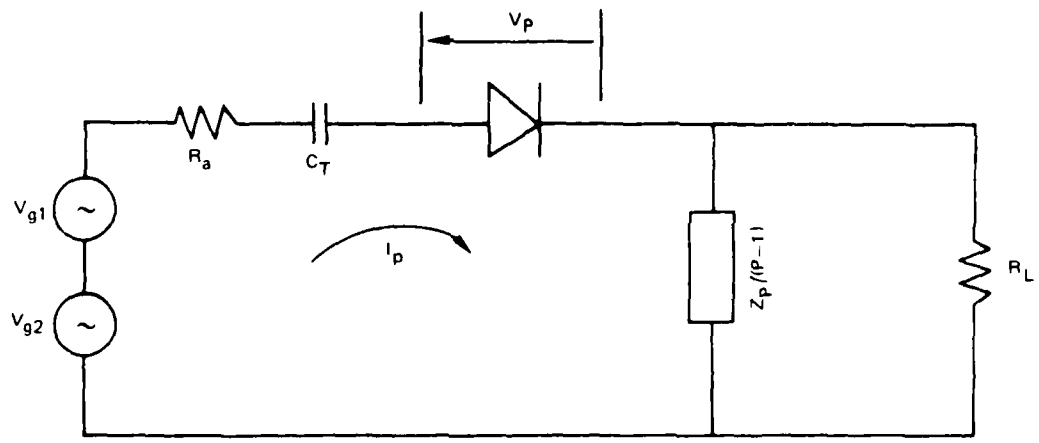
$$G(V_p) \simeq G_0 + G_1 V_p . \qquad \text{(II-17)}$$

The quantities G_0 and G_1 are respectively the diode rf conductance and quadratic coupling coefficient. For diodes that follow the usual exponential I-V characteristic,

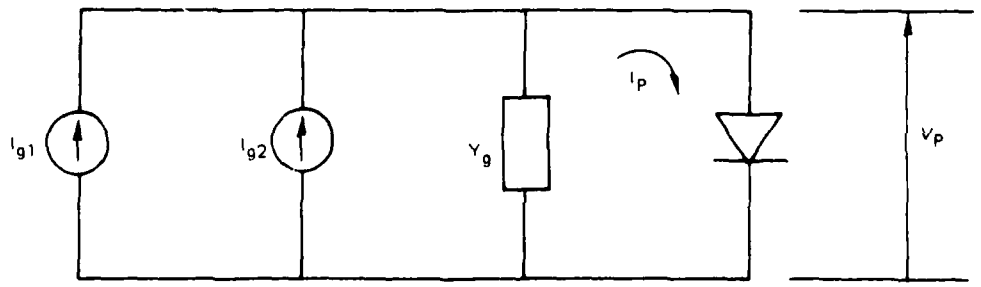
$$G_0 = I_b/V_q \qquad \text{(II-18)}$$

P^{th} DIODE-TAP EQUIVALENT CIRCUIT

a) P^{th} TAP CIRCUIT



b) EQUIVALENT PARALLEL FORM



R03-125-1

$$G_1 = G_0^2/(2\ I_b) \qquad \text{(II-19)}$$

where I_b is the dc bias current at the pth tap, $V_q = \eta kT/q$ is the effective thermal voltage for the diode junction, and η is an empirical factor which is usually near 2 for silicon diodes. A complete nonlinear analysis (Ref. 4) shows that a bilinear transfer function can be written to relate the voltage received at Port 3 due to nonlinear coupling at the pth tap. Assuming that difference frequency operation is used, the relation is

$$V_{p3} = H_{p3}\ V_{g1}\ V_{g2}^* \qquad \text{(II-20)}$$

where

$$H_{p3} = \frac{R_0^2\ R_L/2V_q}{(Z_{p1} + Z_{L1})(Z_{p2} + Z_{L2})(Z_{p3} + PR_L)} \qquad \text{(II-21)}$$

and

$$R_0 = 1/G_0\ , \qquad \text{(II-22)}$$

$$Z_{pi} = R_a(\omega_i) + 1/j\omega_i C_T + R_0\ , \qquad \text{(II-23)}$$

$$Z_{Li} = [1/R_L + (P-1)/Z_{pi}]^{-1}\ . \qquad \text{(II-24)}$$

The magnitude of the generator voltages V_{g1} and V_{g2} can be related to the acoustic power levels incident on the pth tap at frequencies f_1 and f_2,

$$|V_{gi}| = \sqrt{4\ R_{ai}\ P_{ai}}\ . \qquad \text{(II-25)}$$

In turn, the acoustic power levels can be related to the Port 1 and 2 input power levels through the input transducer conversion loss ratios, L_i,

$$P_{ai} = P_i/L_i\ . \qquad \text{(II-26)}$$

Equations (II-18) through (II-26) provide a complete first order model for estimating the variation of DFT voltage output as a function of PDC fixed parameters and the adjustable diode bias current.

Variation of DFT Output as a Function of Diode Bias Current

The maximum DFT output is seen from Eq. (II-20) to occur at the maximum of the bilinear transfer function H_{p3}. The variation of H_{p3} versus bias level can be easily seen by noting that Z_{pi} will be much larger than Z_{Li}, that the tap radiation resistance R_{ai} is typically much smaller than the tap reactance $X_i = -1/\omega_i C_T$, and PR_L is usually much larger than X_3. Thus, to a good approximation

$$H_{p3} \cong \frac{R_0^2 \, R_L/2V_q}{(R_0 + jX_1)(R_0 + jX_2)(R_0 + PR_L)} \quad . \qquad \text{(II-27)}$$

For bias currents sufficiently large, R_0 will be much smaller than X_1, X_2 or PR_L. Thus, for large bias currents Eq. (II-27) becomes

$$H_{p3} \cong -R_0^2/(2PX_1X_2V_q) \simeq K/(I_t)^2 \qquad \text{(II-28)}$$

which says that the DFT output will vary inversely with the square of the pth tap bias current.

The maximum value of DFT output versus bias level can be found approximately by differentiating Eq. (II-27). The value of R_0 at this point is found to be

$$\hat{R}_0 = [2PR_L X_m^2]^{1/3} \qquad \text{(II-29)}$$

where X_m is the tap reactance at the mean frequency $f_m = (f_1 + f_2)/2$. Substituting Eq. (II-29) into Eq. (II-27) gives $\hat{H}_{p3}$ near $1/(2PV_q)$.

To find the absolute value of maximum DFT output we must estimate the maximum values of the tap voltage generators V_{g1} and V_{g2}. These voltages increase with the square root of incident acoustic power until diode saturation begins; very little increase is seen for power levels above the diode saturation point. Since diode saturation occurs near the point where the diode ac current equals the dc bias current, we can use the Fig. II-4 circuit to estimate that the diodes will saturate when the acoustic power level increases to

$$P_{as} \cong V_q^2/(4 \, R_{am}) \qquad \text{(II-30)}$$

where R_{am} is the mean tap radiation resistance. Thus, from Eqs. (II-20, -25) we conclude that the maximum DFT output voltage due to one of the P taps will be close to $\hat{V}_{p3} \cong V_q/2P$.

Dynamic Range

The maximum output dynamic range may be estimated by comparing the maximum DFT output with the expected noise level. The maximum DFT output will occur when all taps are biased to the optimum value specified by Eq. (II-29). From the above analysis we conclude that the maximum DFT power output should be near

$$\hat{P}_3 \cong (\hat{PV}_{p3})^2/2R_L \cong V_q^2/8R_L . \qquad \text{(II-31)}$$

On the other hand, the maximum noise power delivered to Port 3 from the forward biased diode array should not be more than (Ref. 4)

$$\hat{P}_n \simeq 1.5\ kTB \qquad \text{II-32)}$$

where k is Boltzman's constant and T is the absolute temperature. We shall define the tap dynamic range as

$$DR = \hat{P}_3/\hat{P}_n = V_q^2/(12\ kTBR_L) . \qquad \text{(II-33)}$$

For room temperature operation with silicon diodes, a 50 ohm load and 10 MHz bandwidth, the parameters in Eq. (II-33) will be close to V_q = 40 mv, R_L = 50 Ω, and kTB = 3.98 x 10^{-11} mw, giving DR = 78 dB. Thus, the tap dynamic range will typically be greater than 60 dB for PDC modules.

Maximum Fourier Bandwidth

In common with other discretely tapped signal processing devices, the PDC DFT module will be limited to a maximum Fourier bandwidth determined by the sampling rate established at the tapped interaction region. Since the maximum frequency that can be sampled unambiguously by taps spaced ΔT apart is approximately $f_{max} \cong 1/2\Delta T$, we assume that the maximum Fourier bandwidth will be the same,

$$B_{max} \simeq 1/2\Delta T. \qquad \text{(II-34)}$$

To illustrate the maximum Fourier bandwidth that could be obtainable from Eq. (II-34), consider the case of a lithium niobate PDC device with taps separated by 0.001 inch or 25.4 x 10^{-6} m. Since the SAW velocity for Y cut, Z directed lithium niobate is 3488 m/s, we expect ΔT = 7.28 ns and B_{max} = 69 MHz.

E. Analysis of DFT Errors Arising from PDC Tap Amplitude and Phase Tolerance

An estimate of the errors arising in DFT output due to PDC tap amplitude and phase variations can be obtained by computing Eq. (II-12) for the case where the tap amplitudes or phases have a pseudo-random variation. We have done calculations here on a specific PDC example: a 32 tap module with signal processing length T = 1 μs. To assess the error for tap amplitude variations, we have given the real tap weights g_p the form

$$g_p = 1.0 \pm \delta_p \qquad \text{(II-35)}$$

where δ_p is chosen from a random number generator to have a pseudo random, gaussian distribution amplitude from 0 to $\hat{\delta}$. Figure II-5 compares the 32 tap module DFT output for Fourier bandwidth B = 10 MHz with the DFT error computed for $\hat{\delta}$ = 0.0116 and 0.0593 which correspond to dB amplitude variations of 0.1 and 0.5 dB. The DFT error versus output time variable shown in Fig. II-5 is computed by substracting the ideal, error free DFT output from the output including error. As shown in Fig. II-5b and -5c, the average DFT error is close to the pseudo-random tap amplitude error.

To assess the effect of tap phase errors, we have computed Eq. (II-12) for the case where the tap sampling time t_p is given by the following modified version of Eq. (II-5),

$$t_p = (\Delta T/2)(2p-P+1) + \gamma_p \Delta T. \qquad \text{(II-36)}$$

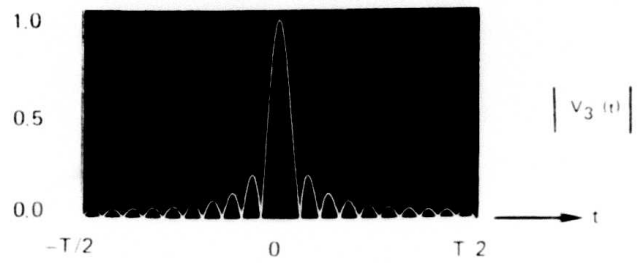
Thus, we have assumed that the tap phase error is equivalent to a pseudo-random tap position error. With the definition used in Eq. (II-36), γ_p corresponds to a fraction error in intertap transit time. Figure II-6 compares the 32 tap module output for B=10 MHz with the DFT error output computed for $\hat{\gamma}$ = 0.01 and 0.02. Here, as in the amplitude case, we note that the average DFT error is comparable to the fractional variation of the tap parameter under study.

The above calculations provide a good rule of thumb for DFT errors: the average DFT error will be near the maximum of δ and γ. However, for most experimental devices, the effects of amplitude error are likely to be much larger than phase errors. This is because amplitude errors on the order of 0.05 to 0.1 dB are quite common in SAW devices while phase errors tend to be much less due to the fine precision available in photolithographic fabrication. For example, consider a device fabricated with taps spaced by 0.001 inch (25.4 μm). The error in tap position over 32 taps should not be more than 0.5 μm giving a maximum phase tolerance of $\hat{\gamma}$ = 0.0006. This tolerance is 16 times smaller than the $\hat{\gamma}$ = 0.01 example computed in Fig. II-6b.

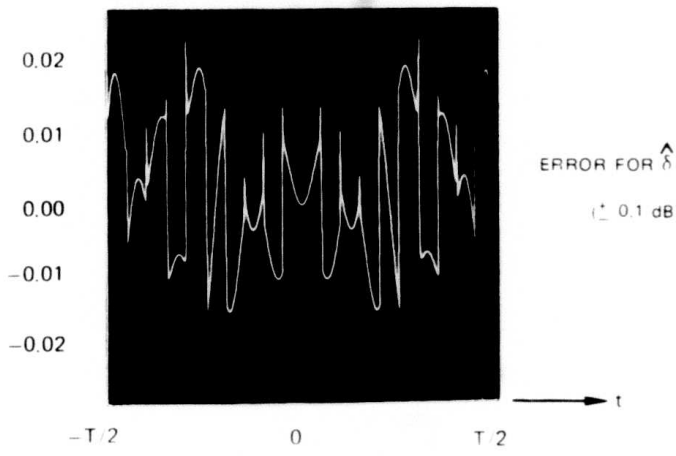
CALCULATION OF DFT ERRORS DUE TO TAP AMPLITUDE TOLERANCE IN A 32 TAP PDC DFT MODULE

(B = 10 MHz, T = 1.0 μs)

a)



b)



c)

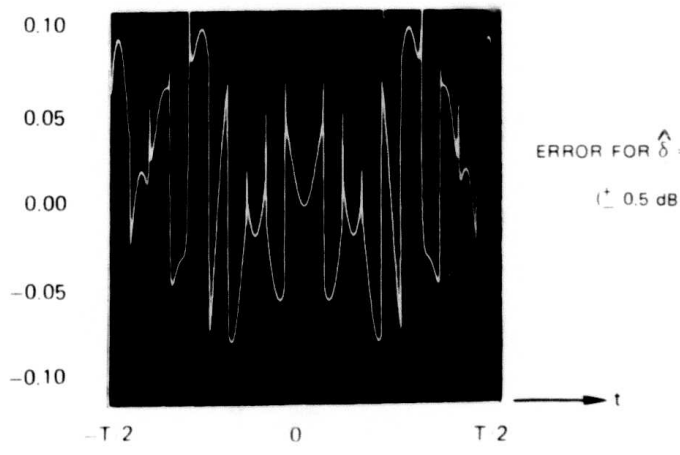
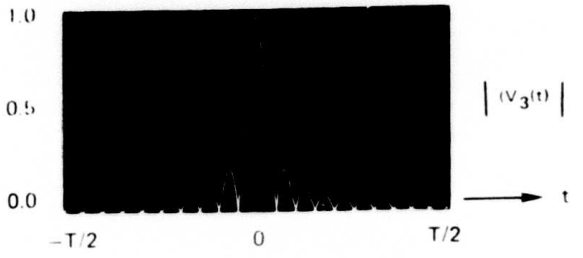


FIG. II-6

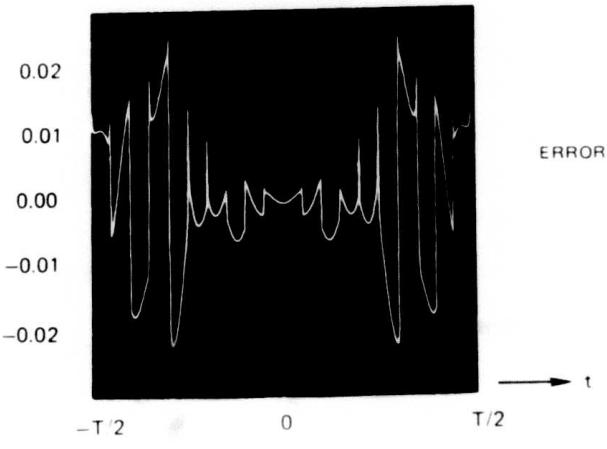
CALCULATION OF DFT ERRORS DUE TO TAP PHASE TOLERANCE IN A 32 TAP PDC DFT MODULE

(B = 10 MHz, T = 1.0 μS)

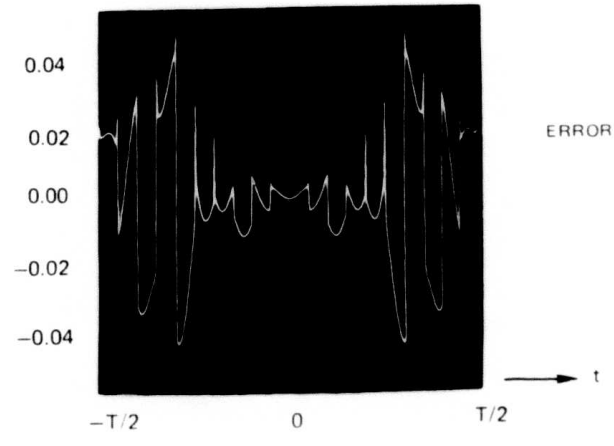
a)



b)



c)



III. OPERATION OF EXPERIMENTAL DFT MODULES

A. Introduction

Two experimental PDC DFT modules were studied during this program; both used Y-cut, Z-directed lithium niobate SAW delay lines. As shown by the summary of physical parameters listed in Table III-1, the two modules used quite different tap configurations. Modules A had 12 taps spaced by 0.1 inch (0.728 μs) while Module B had 32 taps spaced by 0.005 inch (36 ns). Module A used 1N914 discrete diodes: Module B used an IC array of silicon-on-sapphire diodes. Both units were designed to be plugged into an external bias box which allowed the bias to individual diodes to be adjusted independently over a 10:1 range. Figure III-1 shows a diagram of the circuit used for experimental test. The chirp signals applied to Ports 1 and 2 were generated by a Kruse Electronics Model 5000/5010 solid state sweeper operating in the 550 to 600 MHz range. This sweep signal was split into two channels and mixed down to PDC frequencies f_1 and f_2 by use of two stable mixer circuits. These signals were passed through time limiting semiconductor switches and then amplified to the desired -60 to +20 dBm power level. The video pulsers 1 and 2 shown in Fig. III-1 allowed the adjustment of delay and chirp duration in each of the Port 1 and 2 input channels. Thus, the uniformity of the PDC interaction region could be traced out by simply setting one channel to a short pulse length (typically 40 ns or 0.5 μs) and the other to a long pulse length (typically 10 or 100 μs).

B. Module A, 12 Tap PDC

Module A was a discrete diode device built during 1973 to illustrate the elementary features of PDC devices. Being an early device, no attempt was made to use refinements such as low coupling, nonreflecting transducer-taps. Reflections between taps were as large as ±2 dB and were the major limitation of this device. Figure III-2a shows the uniformity of the 12 tap interaction region obtained with a 0.5 μs pulse at Port 1 and a 20 μs pulse at Port 2. The first DFT experiments performed with this device used equal tap amplitudes just as is shown in Fig. III-2a. The amplitude of DFT output expected from Eq. (II-13) in this case is seen to vary approximately as

$$V_3(t) \cong \frac{\sin 2\pi Bt}{2\pi Bt} \quad . \qquad \text{(III-1)}$$

The general form of this variation is seen in the experimental DFT output shown in Fig. III-2b for B = 0.375 MHz. The time width to the nulls of the central sinx/x lobe is 2.7 μs which it should be form Eq. (III-1). However, the sidelobes are not symmetrical due to the inter-tap reflection problem. However, Module A did have high output and large dynamic range (> 60 dB) as can be assessed by the low noise DFT output.

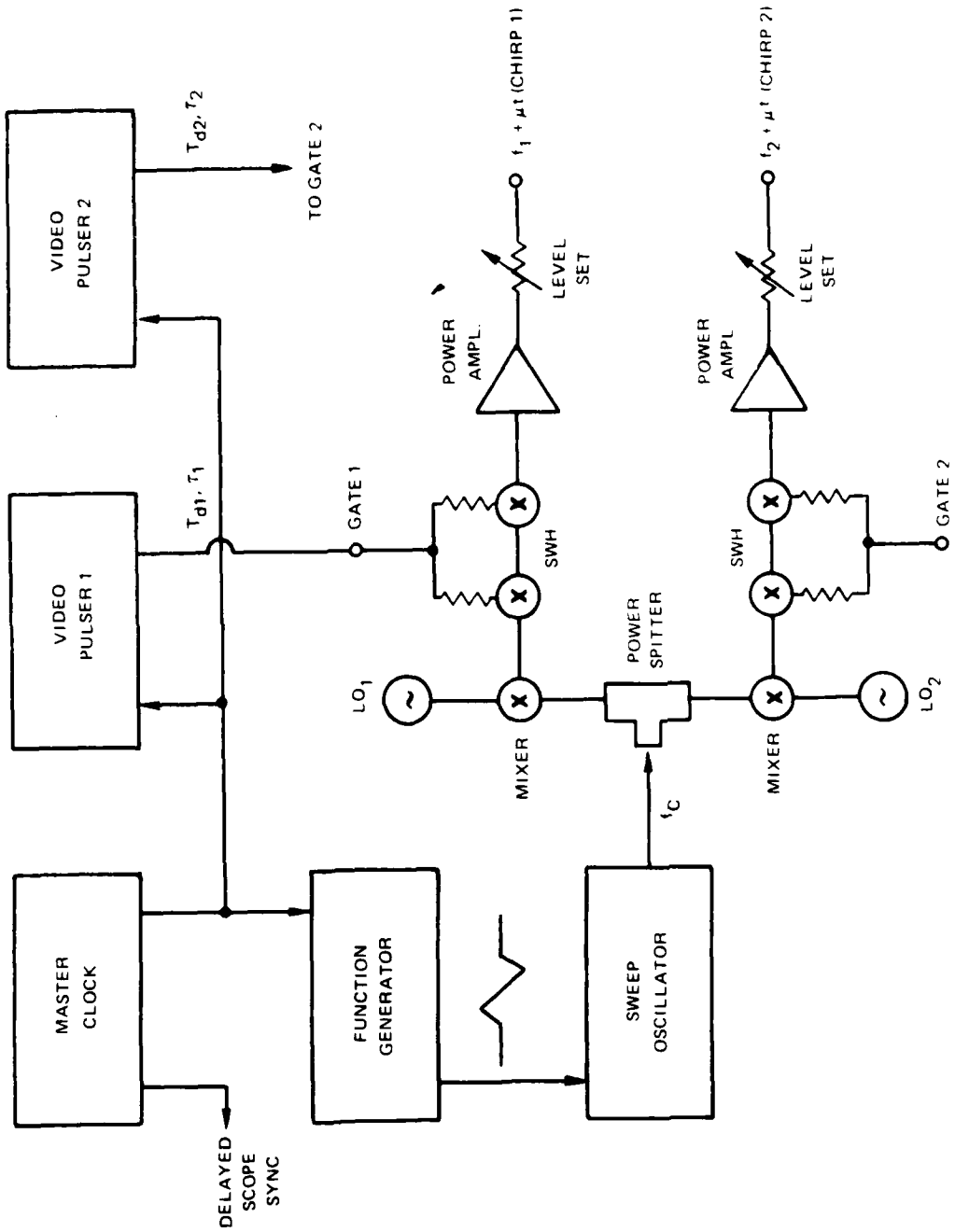
TABLE III-1

Physical Parameters of PDC DFT Modules A and B

Parameter	Module A	Module B
Delay Line	YZ $LiNbO_3$	YZ $LiNbO_3$
Tap Spacing	0.100 inch (0.728 μs)	0.005 inch (36.4 ns)
No. Taps	12	32
Diode Type	IN914	SOS
f_1(MHz)	140	120
f_2(MHz)	200	180
f_3(MHz)	60	60
B_{max}(MHz)	0.69	13.7

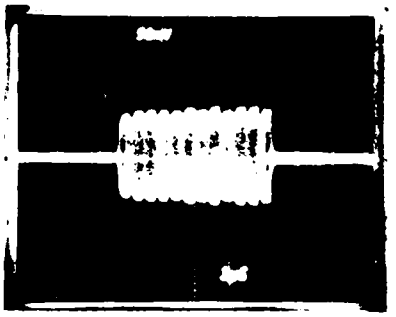
FIG. III-1

REFERENCE CHIRP CIRCUIT UTILIZED IN DFT EXPERIMENTS

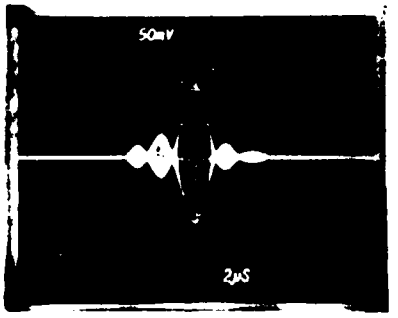


DFT EXPERIMENT WITH MODULE A
(UNIFORM TAP WEIGHTING)

a) DFT OUTPUT WITH SHORT PULSE INPUT (0.5 μs) AND B = 0



b) DFT OUTPUT WITH T = 8 μs AND B = 0.375 MHz



A second DFT experiment was performed on Module A in which the tap amplitudes were adjusted to approximately follow a gaussian shape over the 12 taps. Figure III-3a shows the resultant tap outputs traced out with a short pulse at Port 1 and viewed through a logarithmic amplifier. Figure III-3b shows the DFT output for B = 0.125 MHz and does show the expected gaussian time response.

Detailed measurements were carried out on Module A to verify the variation of DFT versus diode bias current level predicted in Section II. For sufficiently large bias currents, Eq. (II-28) predicts that the amplitude of DFT output should vary as $(I_b)^{-2}$. Experimentally, it was easier to measure the variation of DFT power output P_3(dBm) versus current, and since power is proportional to the square of the output voltage amplitude, the power variation should be proportional to $(I_b)^{-4}$. Figure III-4 compares the DFT output of several different taps of Module A in the case where a short 0.5 μs pulse is applied to Port 1 and the Fourier bandwidth is zero. The data from these taps (and all the rest of the 12) followed the parabolic curve expected from the theory of Section II. For bias currents above 0.4 ma the DFT output did decrease accurately according to $(I_b)^{-4}$. The curves obtained from different taps did agree to within ±3 dB. Since the discrete IN914 diodes used in Module A were randomly selected, this degree of tap output agreement is probably as good as can be expected. Agreement with the theory curve calculated from the measured delay line and diode parameters is also good.

Figure III-5 shows the DFT output of Module A when 10 of the 12 taps were biased on and the input pulses were at least 10 μs. This data gives a conservative measure of the usable dynamic range of the device. The output was still well above noise at -90 dBm and since the maximum DFT output is above -40 dBm, a tap dynamic range near 50 dB is available with this device.

C. Module B, 32 Tap PDC

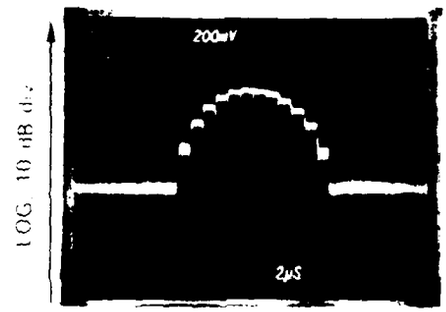
Module B was built to demonstrate the large increase in Fourier bandwidth that is possible in a miniaturized PDC using an IC silicon-on-sapphire diode array. This device used 0.005 inch spacing between taps, giving a maximum unambiguous Fourier bandwidth of 13.7 MHz. Figure III-6 shows a photograph of the Module B interaction region. The SOS diode array with built-in silicon bias resistors can be seen just above the 32 tap delay line interaction region.

Unfortunately, problems were encountered during the fabrication of the silicon-on-sapphire diode array which resulted in a large nonuniformity of diode bias resistor values. This problem was not obvious before assembly because the arrays all looked visually perfect, even though many of the resistors were essentially open circuit. The magnitude of this problem became quite apparent when after several attempts at bonding in nearby diodes to fix diodes known to be inoperative, at least 6 out of 32 taps were still inoperative. Figure III-7 shows a short pulse photo that traces out the uniformity of the 32 tap interaction region.

FIG. III-3

DFT EXPERIMENTS WITH MODULE A
(GAUSSIAN TAP WEIGHTING)

a) DFT OUTPUT WITH SHORT PULSE INPUT (0.5 μs) AND B = 0



b) DFT OUTPUT WITH T 8 μs AND B 0.125 MHz

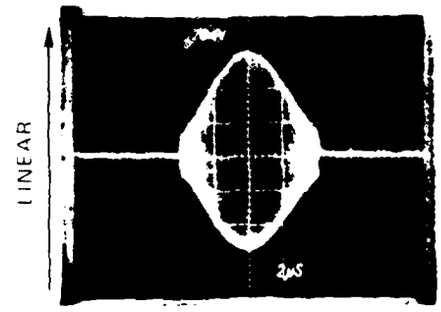
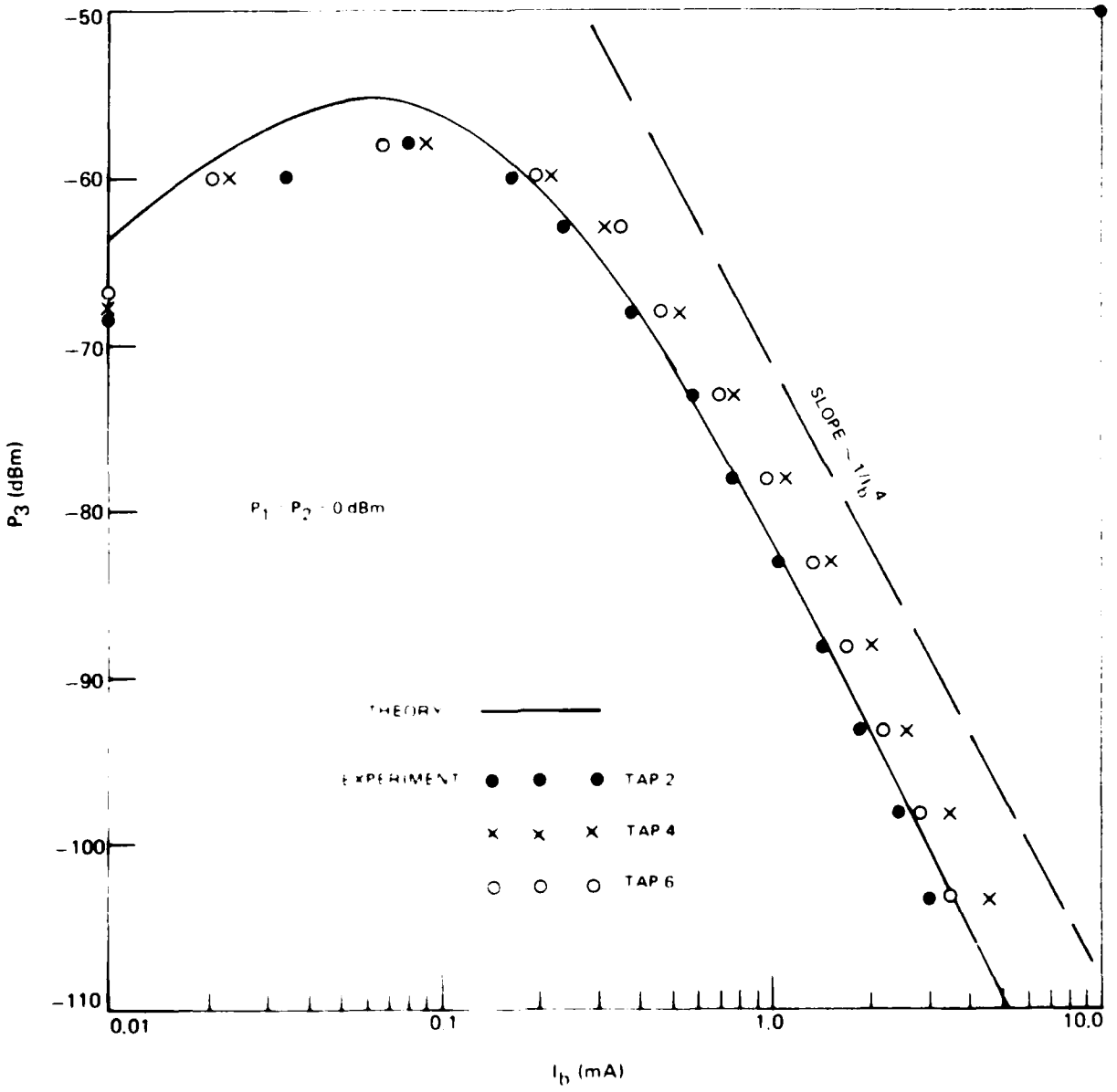


FIG. III-4

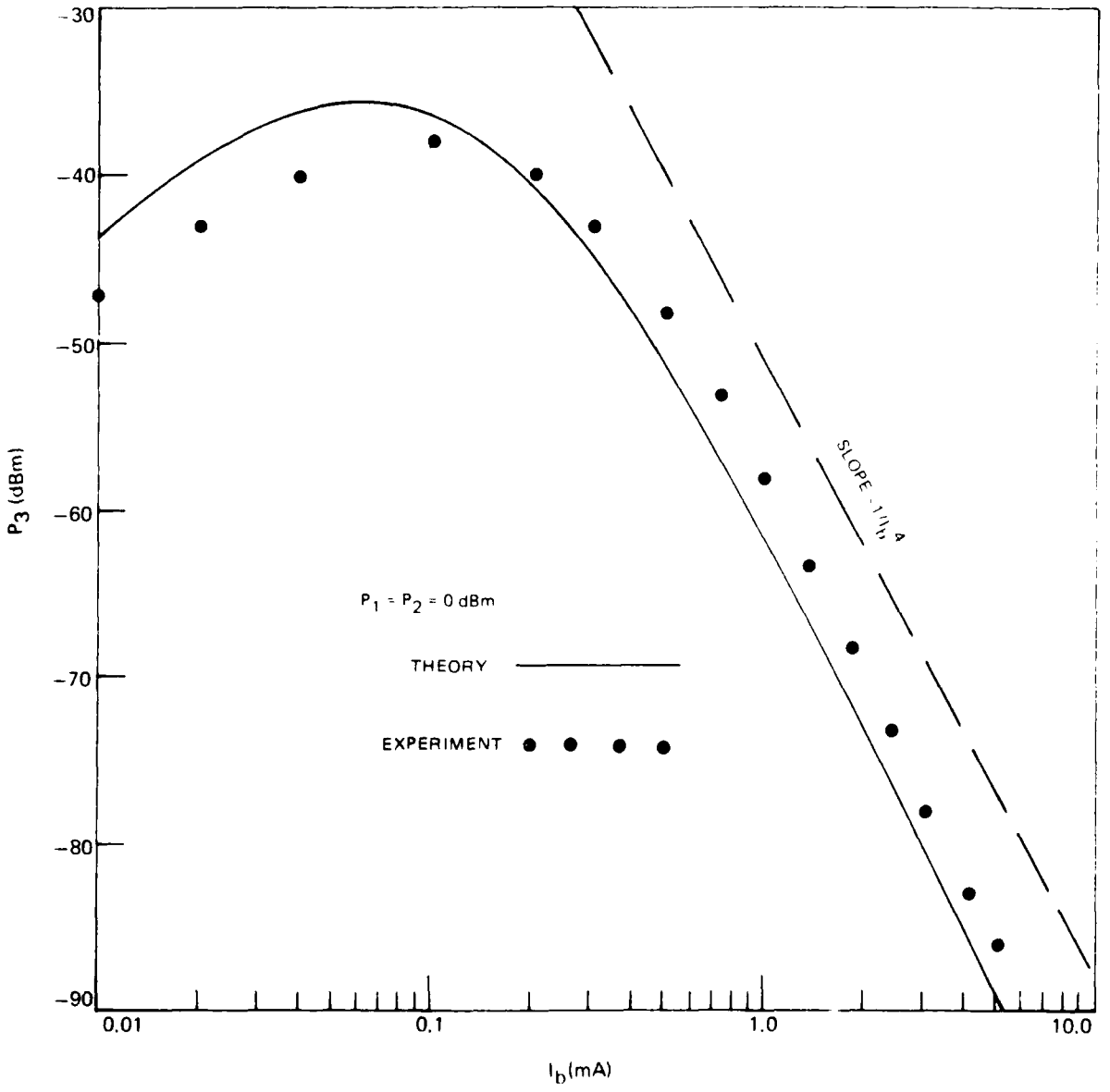
SINGLE TAP OUTPUT VERSUS DIODE CURRENT, MODULE A



N10-282-2

231

10 TAP OUTPUT VERSUS DIODE CURRENT, MODULE A



N10-282-3

FIG. III-6

PHOTOGRAPH OF THE 32 TAP PDC MODULE DELAY LINE INTERACTION REGION

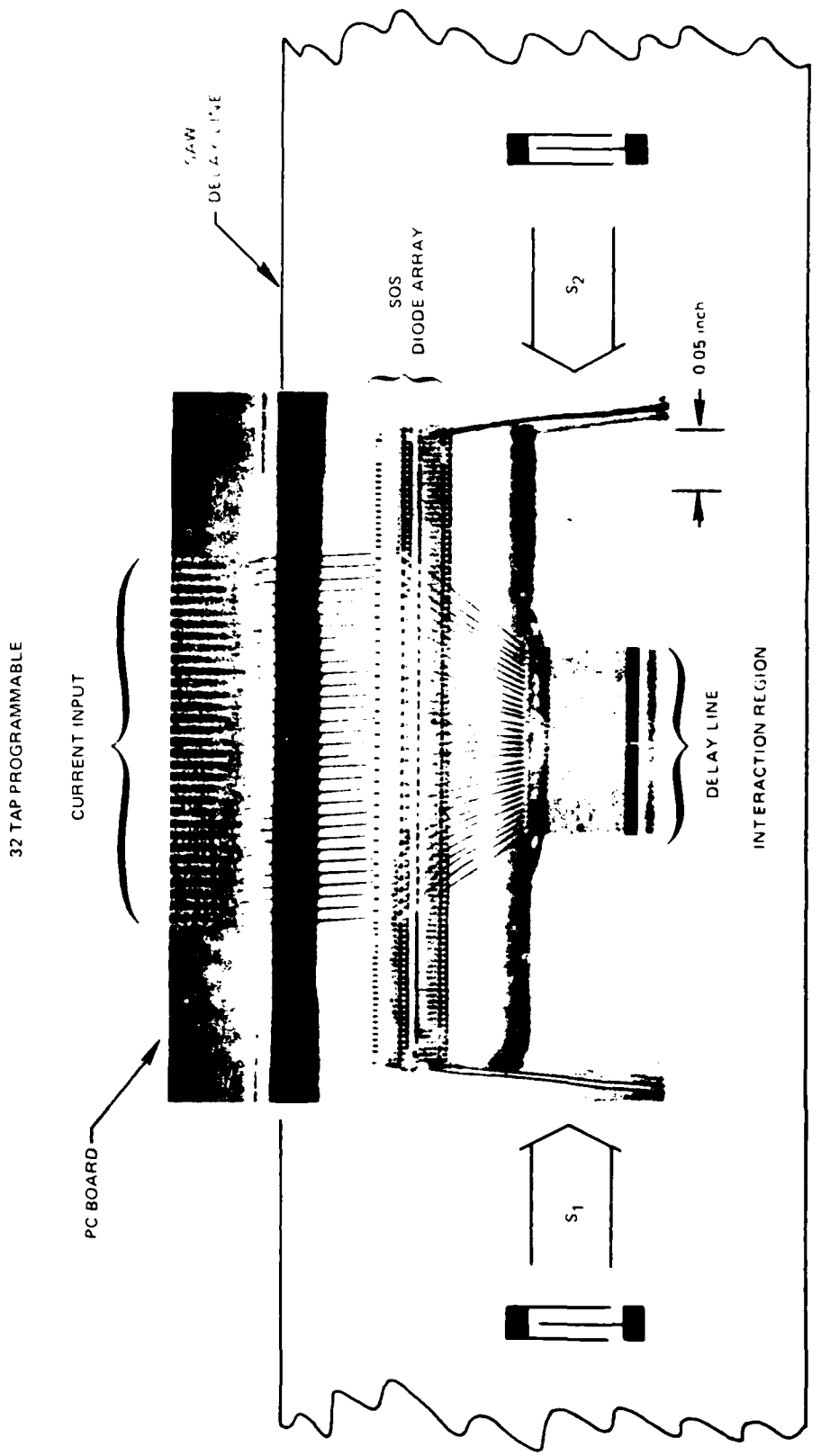
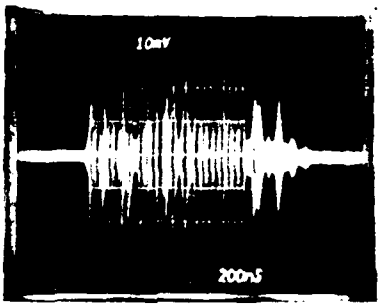


FIG. III-7

DFT OUTPUT FROM MODULE B WITH SHORT PULSE INPUT
(0.04 μ s) AND B = 0

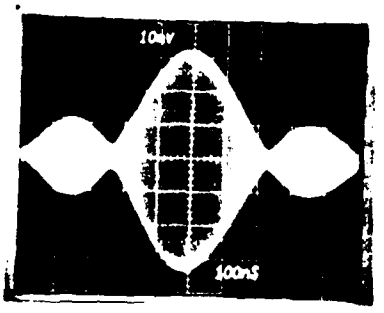


In spite of the fact that 20 percent of the taps did not work, Module B produced very interesting data that does demonstrate the initial feasibility for using the PDC DFT module in wide bandwidth applications. Figure III-8 shows the DFT output obtained as a function of Fourier bandwidth B when all operating taps were biased equally. The expected sinx/x output varied smoothly from B=0 up to and beyond B=5 MHz. Even at B=10 MHz, the near in sidelobes are clearly discernible and at B=20 MHz the central lobe still accurately has the expected 1/B width to the nulls. Thus, the macroscopic features of PDC DFT operation are verified for Fourier bandwidth up to 20 MHz.

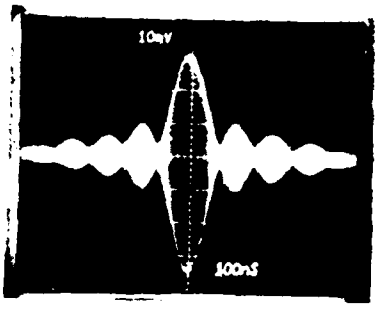
Figure III-9 shows the DFT output from Module B as a function of diode bias current. As before, the data is taken for the case where all taps are biased equally; here we have made the expedient assumption that the individual diode bias current is simply the total current divided by 32. This assumption is certainly in error to some extent since 6 of the 32 taps were not working. However, the resultant plot of P_3(dBm) vs I_b(mA) shown in Fig. III-9 does again follow the $(I_b)^{-4}$ law at high current level ($I_b > 0.2$ mA) and the general shape of the curve is also in agreement with the Module B theory curve shown also for comparison. The biggest discrepancy in the data is, in fact, the relatively low output obtained experimentally. The data is consistently 12 to 15 dB below the calculated curve. Subsequent measurements on the SOS diode array showed that the aluminum metalization was excessively thin, leading to a common line resistance along the diode ground buss of 450 ohms (about 20 times the design value). While unfortunate in the present Module B, such resistance can easily be eliminated in future devices. Thus, there is little doubt that modules using SOS diodes can approach the theory curve shown in Fig. III-9. For bandwidths up to 20 MHz DFT bandwidth, these devices should be usable over a P_3 range from at least -90 to beyond -40 dBm.

FIG. III 8

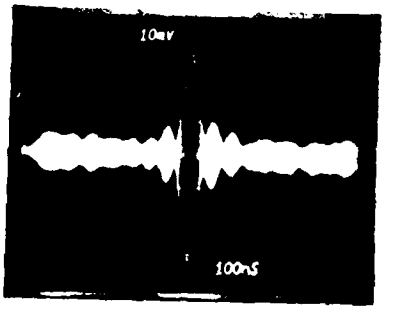
32 TAP DFT MODULE OUTPUT AS A FUNCTION OF CHIRP BANDWIDTH (ALL TAPS EQUAL AMPLITUDE)

a) 

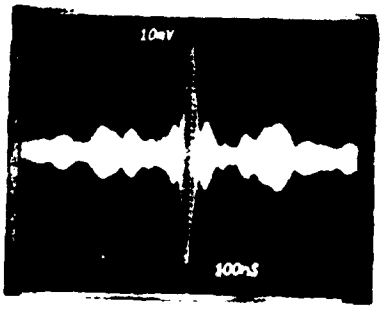
B = 2 MHz

b) 

B = 5 MHz

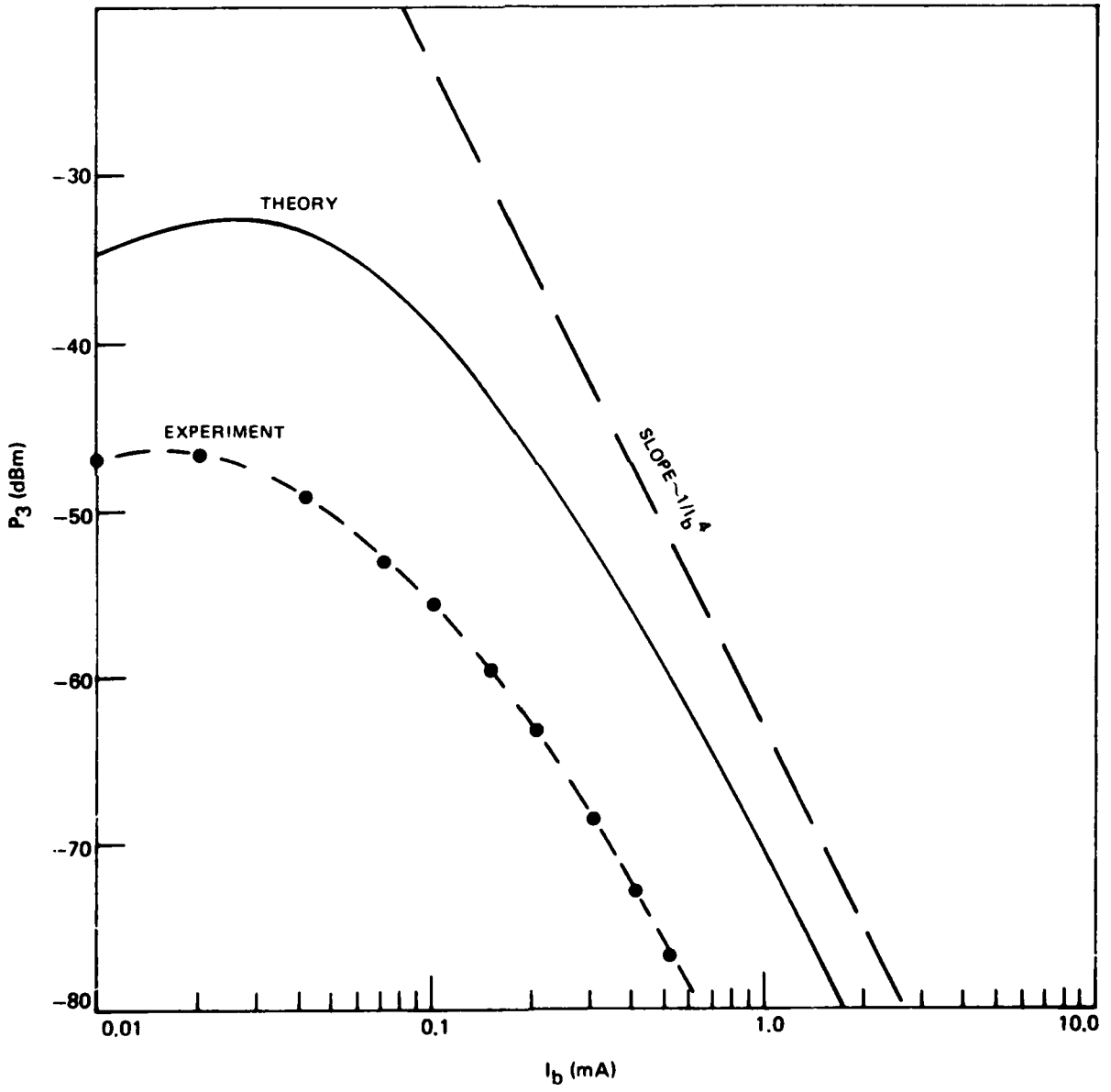
c) 

B = 10 MHz

d) 

B = 20 MHz

DFT OUTPUT FROM MODULE B AS A FUNCTION OF DIODE BIAS (UNIFORM TAP AMPLITUDE, B = 0)



N10-282-1

IV. CONCLUSIONS AND RECOMMENDATIONS FOR FURTHER STUDY

This initial program on DFT modules using the Programmable Diode-Correlator has demonstrated many of the attractive features of these devices: small size, micro-electronic construction, ample dynamic range (> 40 dB), and large Fourier bandwidth (> 10 MHz). Although problems were encountered here in achieving perfect uniformity for the silicon-on-sapphire diodes used in Module B, it seems clear that such problems can be eliminated by refinements in SOS processing, because the dimensions of diode array used in a wide bandwidth unit will always be small (< 0.25 inch).

The variation of DFT voltage output as a function of diode bias was found theoretically and experimentally to vary approximately as $(I_b)^{-2}$. Since the input sampling and first stage transform units will typically provide a tap driving current that is linearly related to the input voltage waveform, the $(I_b)^{-2}$ tap variation will require a reciprocal square root driver stage if a completely linear output transform is to be obtained. The effect of this $(I_b)^{-2}$ variation should be considered in the design of the complete DFT module; an $(I_b)^{-2}$ variation is not necessarily bad because it implies that an input of limited dynamic range could be converted to a dynamic range almost twice as large.

In our view, the PDC DFT is ready for a detailed research and development program aimed at producing modules of extremely precise characteristics. With further detailed processing of the silicon-on-sapphire diode arrays, there is good reason to believe that PDC DFT modules with near perfect characteristics can be achieved. For example, 32 or even 64 tap devices with tap spacings as small as 0.001 inch and amplitude uniformity within 0.1 dB appear feasible. The result would be a parallel input-serial output DFT modules with at least 50 MHz Fourier bandwidth.

V. REFERENCES

1. Reeder, T. M. and M. Gilden: Convolution and Correlation by Nonlinear Interaction in a Diode Coupled Tapped Delay Line, Appl. Phys. Lett., 22, 8-10, (January 1, 1973).

2. Reeder, T. M.: Insertion Loss and Saturation Effects in the Diode-Correlator, Electronic Letters, 9, 254-256, (May 31, 1973).

3. Reeder, T. M.: Electronically Variable Chirp Signal Correlation with the Diode Correlator, IEEE Intern'l. Microwave Symp. Digest, 237-239, (June 1974).

4. Reeder, T. M. and J. L. Swindal: Variable Acoustic Surface Wave Correlator, Technical Report ECOM-73-C-0194, U. S. Army Electronics Command, Ft. Monmouth, N. J., (September 1974).

5. Speiser, J. M., H. J. Whitehouse, and J. M. Alsup: High Capacity Linear Processing Using Multidimensional Chirp-Z Transforms, NUC TN 1212, Naval Undersea Center, San Diego, California, (13 Nov. 1973).

6. Speiser, J. M. and H. J. Whitehouse: The Modular Chirp-Z Transform, NUC TN 1355R, Naval Undersea Center, San Diego, California (May 1974).

7. Speiser, J. M. and H. J. Whitehouse: The Modular Chirp-Z Transform, National Telecommunications Conf., 1974 Record, 259-262.

8. Wintz, P. A.: Transform Picture Coding, Proc. IEEE, 60, 809-820, (July 1972).

9. Image Transmission Via Spread Spectrum Techniques, Technical Report ARPA QR4, Naval Undersea Center, San Diego, California, (January 2 - July 1, 1974).

10. Buss, D. D., et al.: Transversal Filtering Using Charge-Transfer Devices, IEEE Journ. of Solid State Circ. SC-8, 138-146 (April 1973).

11. Kino, G. S., et al.: Signal Processing by Parametric Interactions in Delay Line Devices, IEEE Trans. on Microwave Theory and Tech., MTT-21, 244-254, (April 1973).

12. Mertz, A.: Transformation in Optics, 94-96, Wiley: New York (1965).

13. Rabiner, L. R., R. W. Schafer, and C. M. Rader: The Chirp-Z Transform Algorithm, IEEE Trans. on Audio and Electroacoustics, AU-17, 86-92 (June 1969).

14. Whitehouse, H. J., J. M. Speiser, and R. W. Means: High Speed Serial Access Linear Transform Implementation, All Applications Digital Computer Symposium, Orlando, Florida, (January 1973).

15. Alsup, J. M.: Surface Acoustic Wave CZT Processors, Proc. IEEE Ultrasonics Symposium IEEE 74CH0896-1SU, 378-381 (November 1974).

16. Anderson, G. B. and T. S. Haung: Piecewise Fourier Transformation for Picture Bandwidth Compression, IEEE Trans. on Comm. Tech., COM-19, 50-52, (February 1971).

17. Hibibi, A. and P. A. Wintz: Image Codings by Linear Transformation and Block Quantization, IEEE Trans. on Comm. Tech., COM-19, 50-52 (February 1971).

INTEGRATED MONOLITHIC ANALOG MEMORY DEVICE HAVING RANDOM INPUT ACCESS, ARAM-64

G. Weckler
E. Snow
S. Tanaka
and
R. Buss
Reticon Corporation

INTEGRATED MONOLITHIC ANALOG MEMORY DEVICE HAVING RANDOM INPUT ACCESS, ARAM-64

G. Weckler, E. Snow, S. Tanaka and R. Buss

FORWORD

This development effort was authorized by Contract N66001-75-C-0204 EDS, issued by the Naval Undersea Center, San Diego, California. This report covers the entire work of the contract during the period May 12, 1975, through October 17, 1975.

Mr. H. Whitehouse directed the work herein for the Naval Undersea Center.

ABSTRACT

A random-input-access, serial-output analog memory device, ARAM-64, has been successfully developed. Sample rates to 5MHz with a dynamic range of 45 db are obtained. The signal transmission loss is approximately 25 db, largely from internal capacitive voltage division. The output circuit includes provision for internal sample-and-hold enhancement of performance.

I. OBJECTIVE AND SCOPE

Reticon Corporation has privately developed and marketed a Serial Analog Memory Device, SAM-64, which sequentially samples an input analog signal and stores those samples on successive memory capacitors. Under separate control, those input samples are successively destructively

read out onto an output signal line. The device thus functions in a manner herein described as a serial analog memory. The objective of the contract work here described was to develop a similar device in which the memory capacitors were randomly addressable on the input side, so that the order of storage could be arbitrarily selected. High speed of operation, up to 5MHz sample rate, and a large dynamic range were also objectives.

II. IMPLEMENTATION

The method selected for implementation is that of providing an on-chip six-bit binary decoder so that any one of the sixty-four memory cells can be selected by a six-bit input binary address. In addition, a common strobe input is provided so as to minimize erroneous decoding because of relative propagation delays in the multiple address gates.

Fundamentally the principle of its operation is an extension to that of Reticon's serial analog memory (SAM) devices. The SAM contains an input shift register which sequentially selects the memory cells to store discrete samples from the input signal line and an output shift register which sequentially selects the memory capacitors to read out on the output signal line.

In contrast to the SAM, the input switches of the new device are controlled by a one-out-of sixty-four CMOS binary logic decoder. Six parallel address lines receive and transmit the binary-coded information to the decoder which selects and activates a particular switch to a

memory storage cell. The standard shift-register control of the read out sequence is retained, as in SAM-64, but the output is split into two separate channels. One (the odd channel) is multiplexed to odd-numbered storage cells, and the other (the even channel) is multiplexed to even-numbered storage cells. Further, each channel is provided with an MOSFET shunt switch and with an MOSFET open-source transistor connected as a source follower so as to facilitate a sample-and-hold mode of operation which gives improved performance. The effective schematic arrangement is as shown in Figure 1.

The decoder design uses CMOS technology in order to provide the required operating speed. Further, the decoder gating paths are equalized for propagation delay so as to minimize erroneous transient decoding. A common strobe channel is likewise implemented. The provision of the more extensive gating required to enhance high-speed operation is at the expense of more chip area in the integrated circuit. The operation of the device designed with regard to the above factors is given below in the performance and specifications sections III B and III C.

III. CHARACTERIZATION OF THE DEVELOPED DEVICE

A. Functional Arrangement

The device as developed, designated ARAM-64, has a functional arrangement as shown in Figure 1. It is enclosed in a standard 18-pin dual-in-line package with pin configuration as in Figure 2. The six-bit binary input address is combined by the

logic gates to make an input-signal connection to one and only one storage cell for each logic combination, provided the strobe is enabled. The strobe input may be used to enable or disable the entire input addressing at rates within its limits as defined by the timing diagram, Figure 6.

Figure 3 is an enlarged schematic to show details of the input and output signal lines and their connections through the control switches to the odd-numbered and even-numbered memory capacitors. Each output line is buffered by means of an FET source follower, and each line has a reset FET shunt switch. The functioning of these devices is further discussed in the following section.

1. Signal Input and Output

Signal input is connected through the input switch from the input line to an arbitrary memory capacitor; thus the impedance looking into the signal input port is a capacitance in shunt with a resistive component. The resistive component is determined by the sampling rate via the activation of the input switches which charges a new memory capacitor with each address change (Figure 3). Because the charge transferred to each capacitor is small, the effective shunt resistance seen on the line is very high.

There are two output signal lines, one for the odd-numbered memory cells and another for the even-numbered cells. Each output line is connected through a set of switches

to their respective odd- and even-numbered memory capacitors and terminated with a buffer FET and connected to a shunt FET switch as shown in Figure 3. This geometry enhances the signal processing implementation by providing a low-impedance output and a means of resetting the voltage on the output signal line after each interrogation of the memory cells. Use of this buffer and shunt switch permits formation of a sample-and-hold circuit.

By inspection of Figure 3 it can be seen that, when a particular cell is interrogated, the stored signal charge is switched out from the memory capacitor onto one of the output signal lines to be integrated and held until the shunt switch is activated, at which time the held information is reset to a given reference level while the next packet of information is held on the opposite output line. Thus the output of this device divides the stored information (approximately the input voltage) by the ratio of memory capacitance to the output-line capacitance which ratio is approximately 1/10. The held output is still further reduced by the non-ideal FET buffer which has a transfer factor or gain in the order of 0.5. This gain depends on the load resistor on the output terminal (Figure 4, Gain Versus Output Resistor). Thus the overall transfer factor involves a loss of approximately 25 db.

2. Output Drive Requirements

Two-phase dynamic shift registers are used for the read-out switches. The low-powered PMOS shift register is clocked from a CMOS complementary driver. The control of the output signal sample rate is obtained by varying the shift-register clock and/or the shift-register start pulse.

Figure 5 depicts a timing diagram which shows the timing relationship between the clock and start pulse. The start pulse loads into the shift register on the rising edge of ϕ_1, hence the start pulse is required to be present only during this setup and hold time with a window width of approximately $\pm$30 nsec around the rising edge. Once the start pulse is loaded, further clock pulses cause a full-width pulse to shift down the register sequentially closing and opening the access switches starting with Cell No. 1. Cell No. 1 is accessed with the fall of ϕ_2 (the same as the rise of ϕ_1). Cell No. 2 is accessed at the next fall of ϕ_1, and so on. The process continues until it terminates after the 64th cell is accessed. The start pulse must then be reloaded to cycle over again; otherwise no cells will be interrogated. Multiple start pulses, or an excessively long start pulse, will cause simultaneous interrogation of more than one memory cell and hence faulty operation. The start pulse input is thus equivalent to the data input to a shift register, but this shift

register transfers the data on every clock transition instead of only once per full clock-cycle.

3. *Input Drive Requirements*

The input switches are controlled by a one-out-of-sixty-four CMOS decoder which is addressed by six address lines and a strobe.

The strobe is active when it is pulled high and inhibits the address line when it is pulled low. The decoding logic selects the particular switch via a binary code applied to the address lines A, B, C, D, E, F, which are all, including the strobe, CMOS inputs requiring similar levels to activate the logic. The logic structure of the decoder is shown in Figure 1. Binary input selection may be varied at the full 5MHz sample rate with the strobe constantly enabled provided the external address control is synchronous; full internal strobe control is limited by switching speed to approximately 1MHz.

B. Performance Data

Performance data were obtained using the simplified circuit shown in Figure 7. This circuit generates the required output clocks, and two versions of an input address code. It may be operated so as to give either FIFO or FILO serial input sequences and includes the required driver circuits. The transfer function of Figure 8 was obtained by using a normal FIFO or continuous delay mode. The performance was measured with a spectrum analyzer with IF

bandwidth approximately 1KHz. The second-harmonic line is shown to give the relative device linearity in terms of second-harmonic generation. The dotted line shows the clock-related spurious signal level which is considered to be the limiting factor at the low end of the dynamic range.

Using this test circuit, the output voltage versus output resistance was measured with a constant input voltage. These data were plotted and shown in Figure 4. From this measurement the approximately 900-ohm output impedance of the device was inferred to apply as indicated over the normal loading range of 1 to 2 kilohms.

C. Specifications

The performance to be expected from the device is summarized in the following specifications where, unless otherwise indicated, all voltages are measured with respect to the common terminal, pin 14, and the data apply to normal room-temperature operation.

IV. CONCLUSIONS

The measured data and specifications indicate successful development of a random-input-access, serial output analog memory in accordance with the contract objectives. Sampling data rates to 5MHz are possible and a dynamic range of approximately 45 db is obtainable.

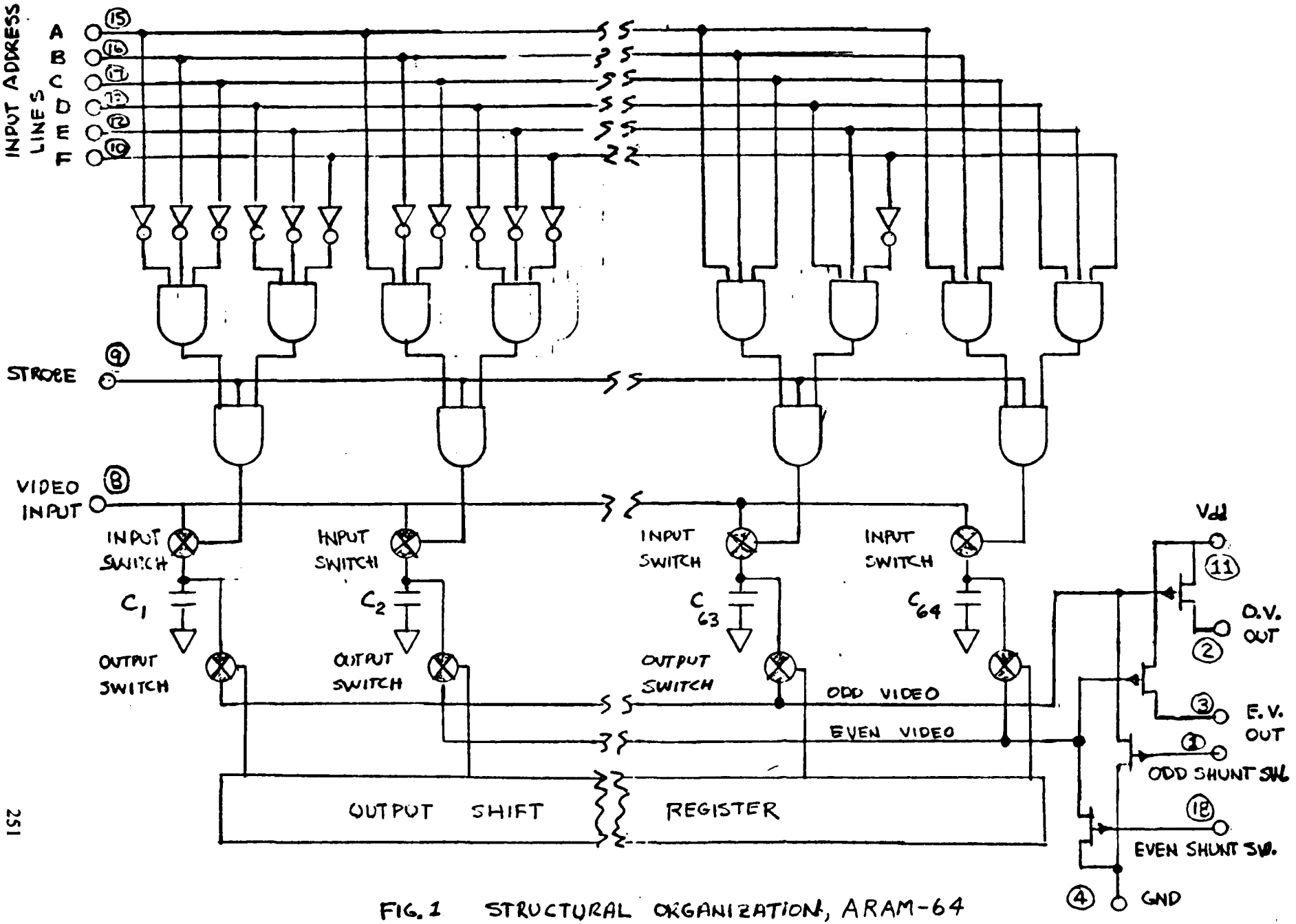


FIG. 1 STRUCTURAL ORGANIZATION, ARAM-64

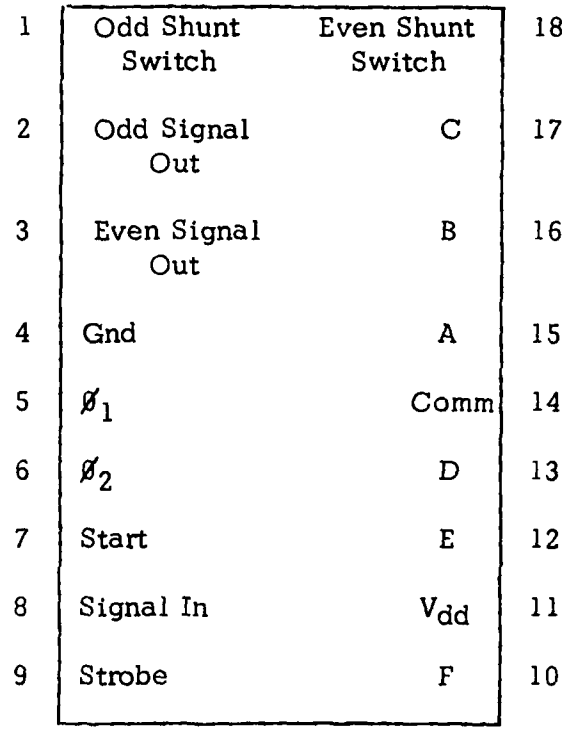
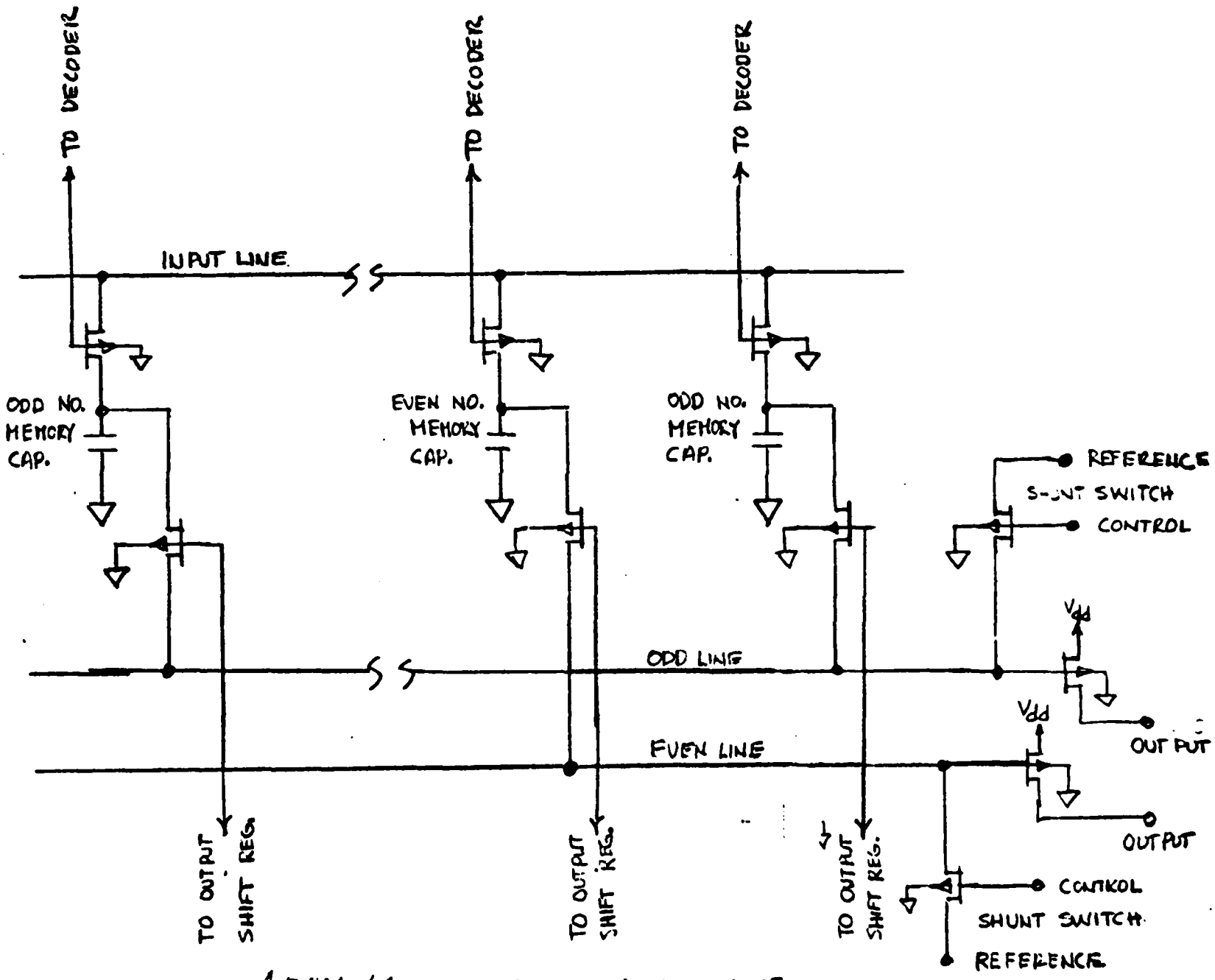
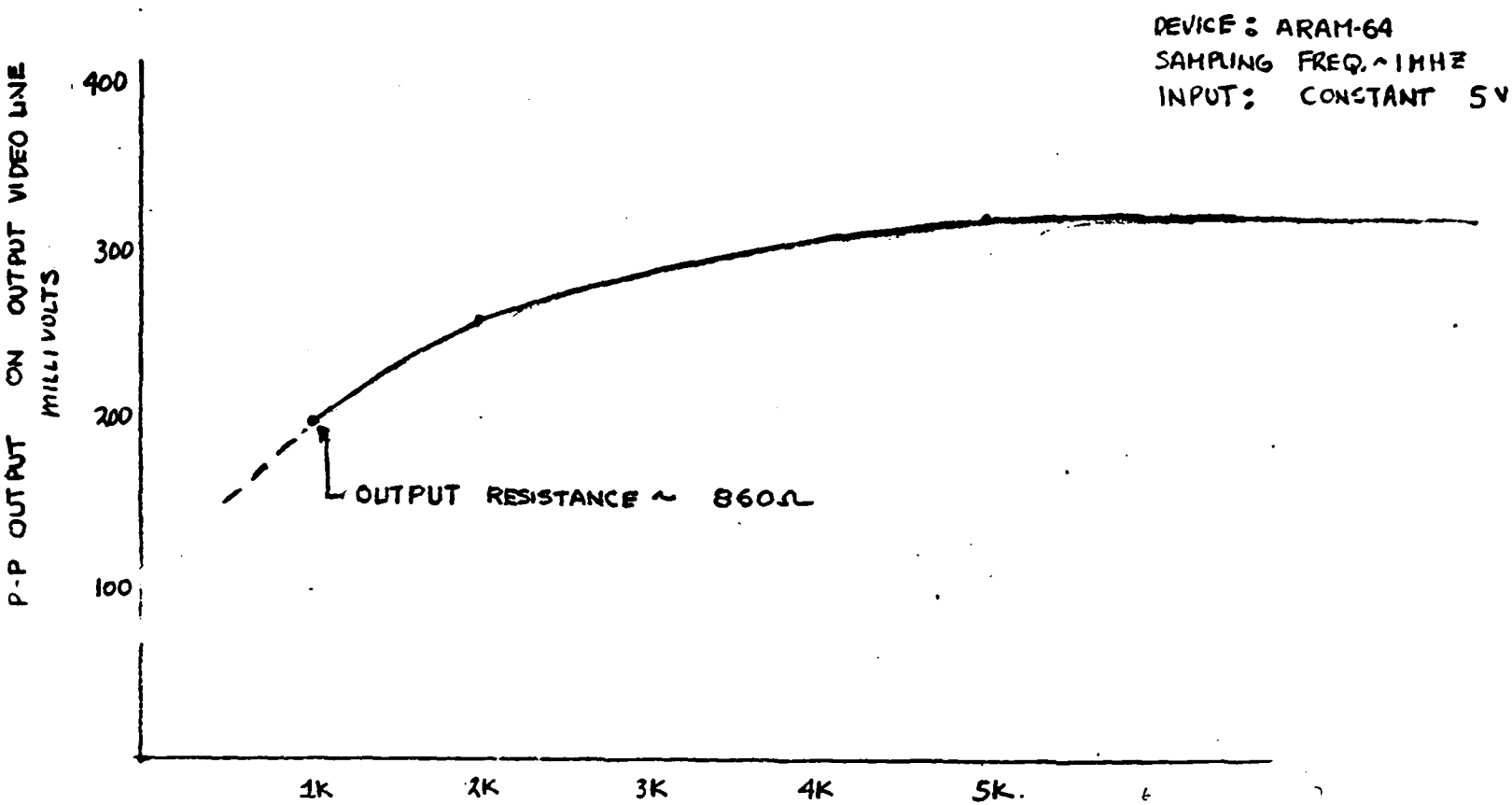


Figure 2. Pin Configuration ARAM-64



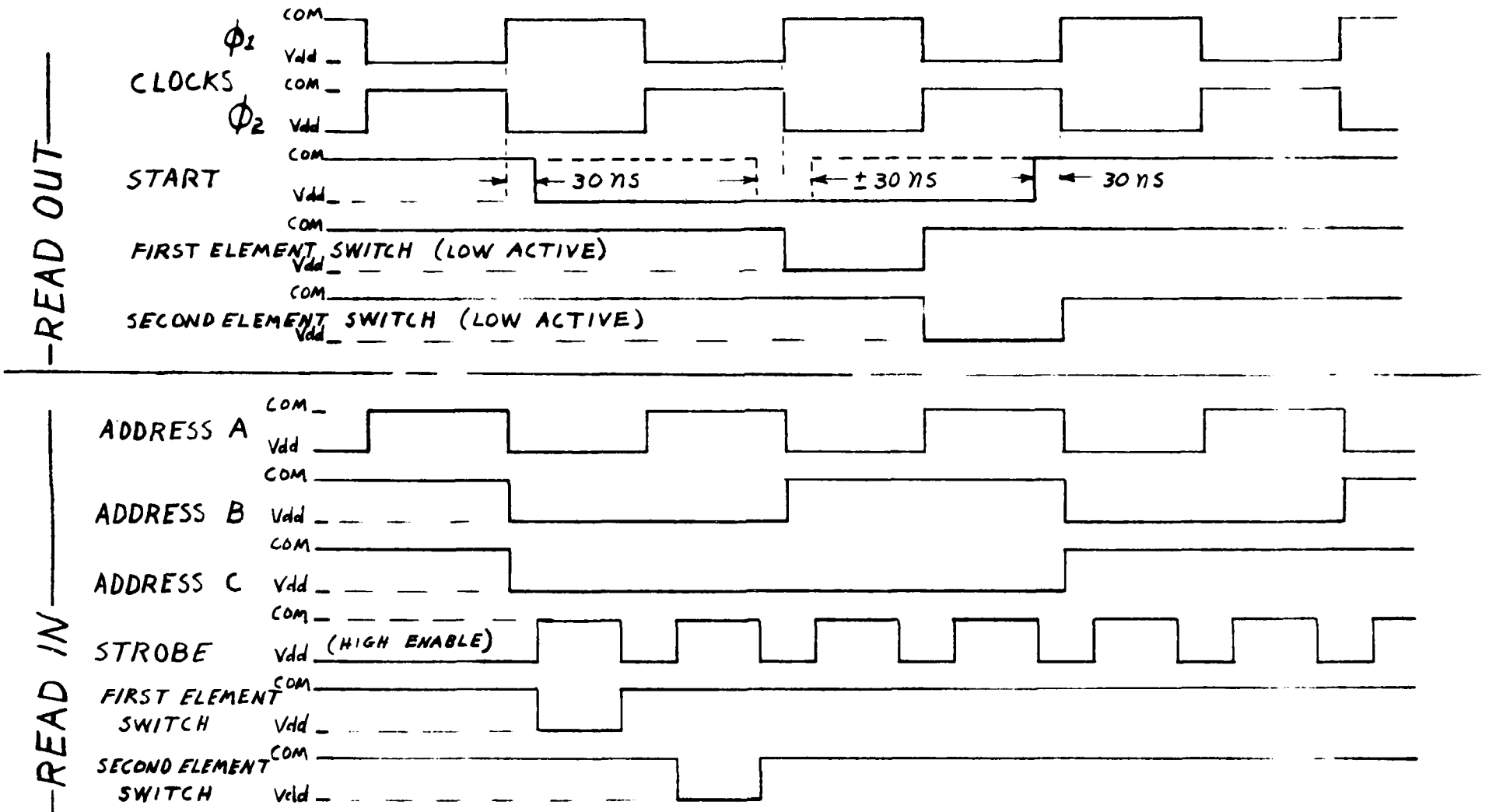
ARAM-64 INPUT AND OUTPUT VIDEO LINE

FIGURE 3



OUT PUT VOLTAGE VS OUT PUT RESISTANCE.

FIGURE 4



NOTE: INPUT SHOWN FOR THREE ADDRESS LINES ONLY.

FIG. 5 DEVICE CLOCKING DIAGRAM FOR READIN AND READOUT

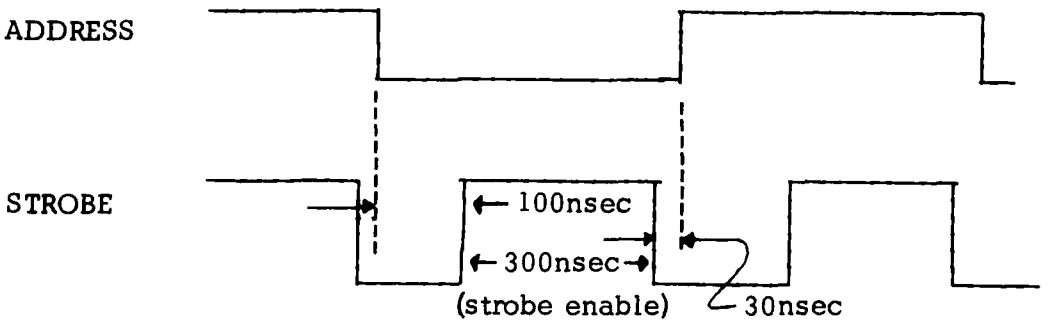


Figure 6. Minimum Timing Requirements for Valid Strobe Control

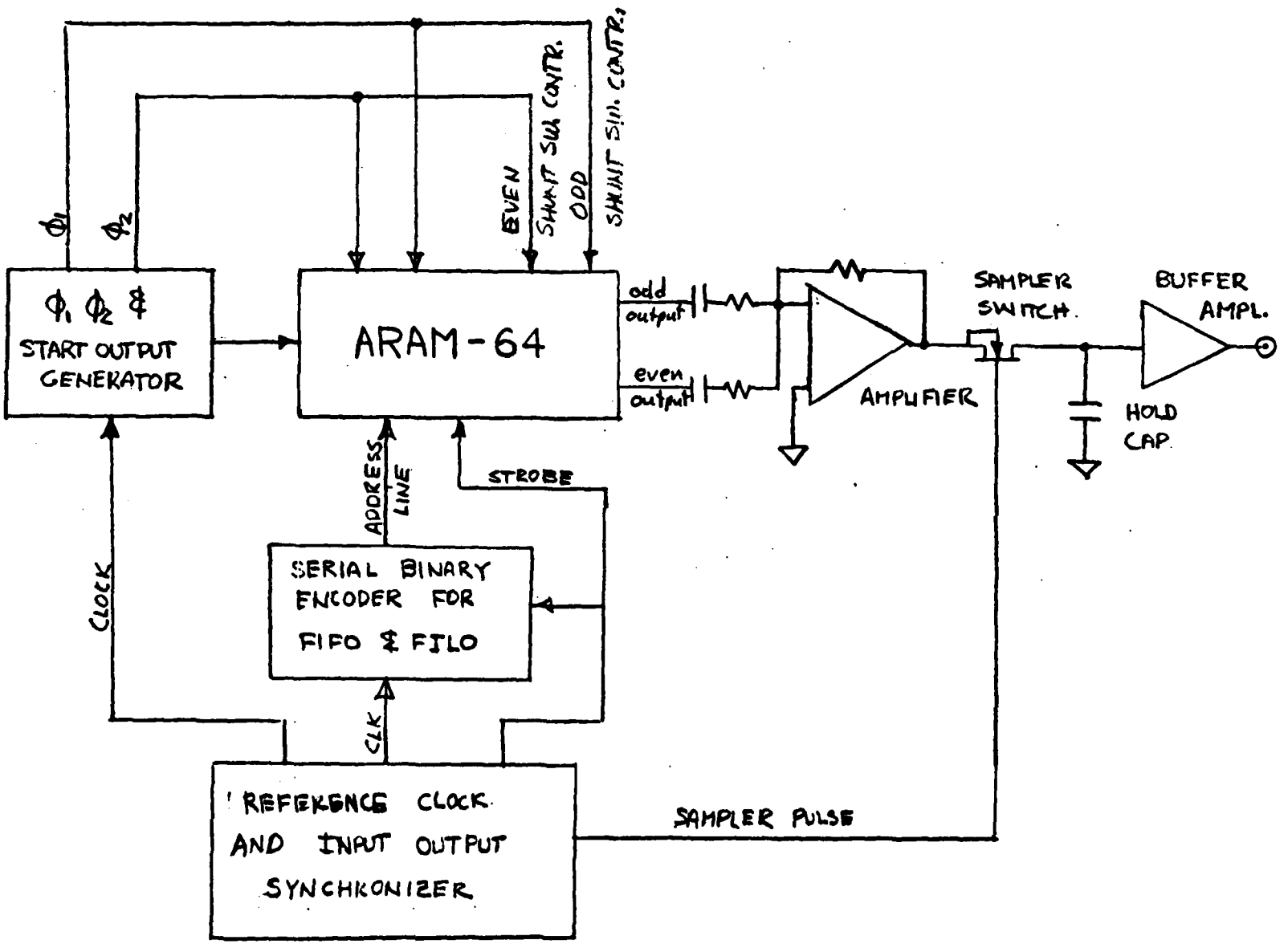
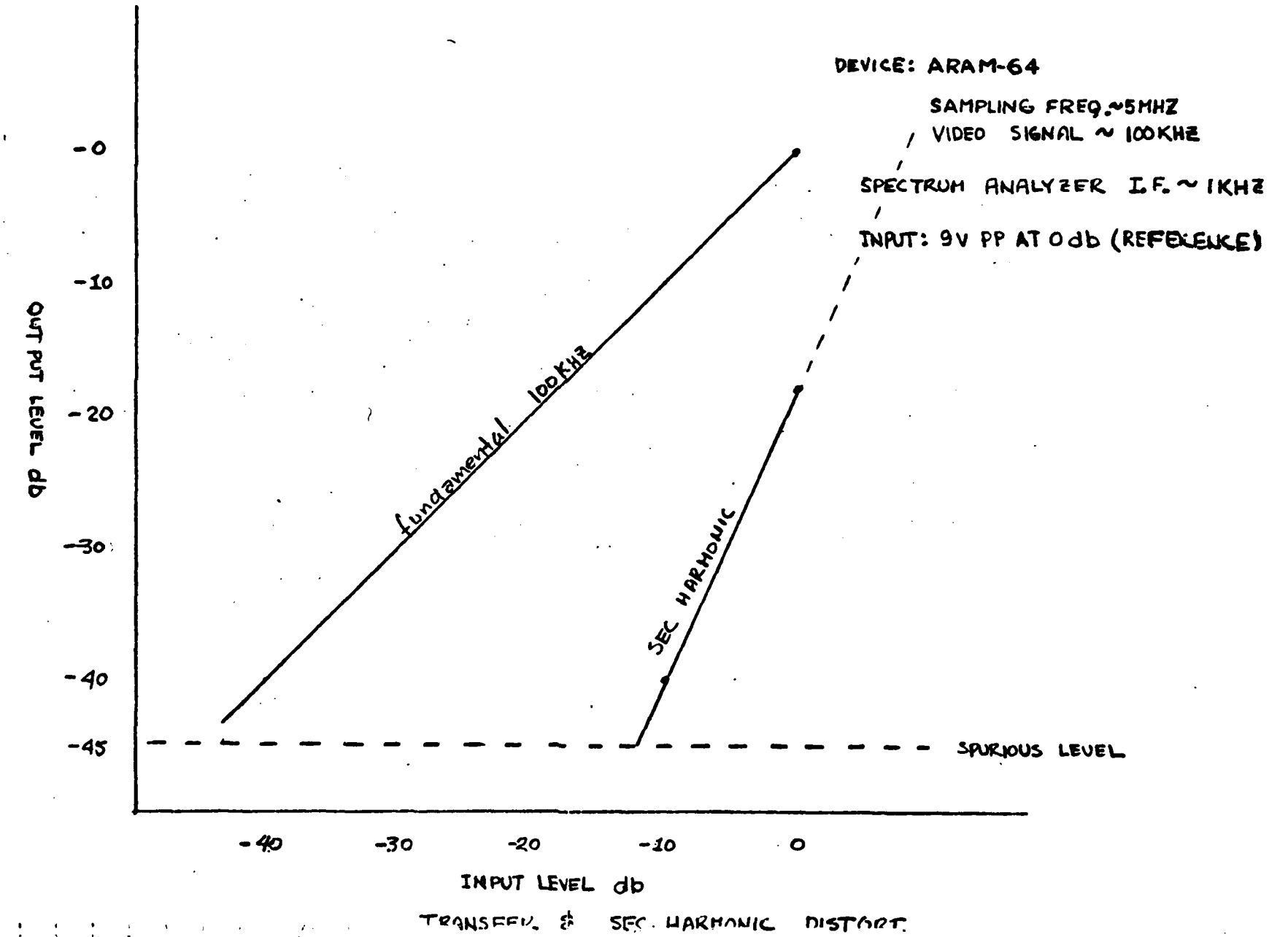

ϕ_1
ϕ_2
EVEN SHUNT SW. CONTR.
ODD SHUNT SW. CONTR.
ϕ_1 ϕ_2 &
START OUTPUT GENERATOR
ARAM-64
odd output
even output
AMPLIFIER
SAMPLER SWITCH.
BUFFER AMPL.
HOLD CAP
ADDRESS LINE
STROBE
CLOCK
SERIAL BINARY ENCODER FOR FIFO & FILO
CLK
REFERENCE CLOCK AND INPUT OUTPUT SYNCHRONIZER
SAMPLER PULSE

FIG. 7.



TRANSFER & SEC. HARMONIC DISTORT.

FIGURE 8

SPECIFICATIONS

ABSOLUTE MAXIMUM VOLTAGES

All Voltages Referred to Common, Pin No. 14

TERMINAL	LIMITS
V_{dd}	+0.4 to -14 volts
ϕ_1 Clock	+0.4 to -14 volts
ϕ_2 Clock	+0.4 to -14 volts
Start	+0.4 to -14 volts
Signal Input	+0.4 to V_{dd}
Even & Odd Signal Out[1]	+0.4 to V_{dd} -0.5 volts
Even & Odd Shunt Switch	+0.4 to -14 volts
Strobe and all Address Lines[1]	+0.4 to V_{dd} -0.5 volts

[1] Voltages outside the limits V_{dd} and common may forward-bias diodes and are to be avoided.

OPERATING PARAMETERS (ALL VOLTAGES REFERRED TO COMMON)

	Max	Norm	Min
Sampling Freq[2]	5MHz		
Supply V_{dd}	-14 volts	-10 volts	
ϕ_1 Clock Amplitude		V_{dd}	
ϕ_2 Clock Amplitude		V_{dd}	
Start Amplitude		V_{dd}	
Clock Rise Time t_r		10nsec	

OPERATING PARAMETERS (Continued)

	Max	Norm	Min
Clock Fall Time t_f		20nsec	
Signal B.W. @ 5MHz sampling rate		1.5MHz @ 3 db	
Signal to Noise Ratio		See Fig. 8	
Gain		See Fig. 4	
Signal Line Output Resistance		860 ohms	
Input Shunt Resistance		50K ohms	
Strobe Voltage Amplitude		$\lvert V_{dd} \rvert$	±0.5 volts

Strobe pulse width, and timing with respect to A Address Line, See Waveform, Figure 6.

All Address Line Voltage Amplitudes[3]		$\lvert V_{dd} \rvert$	±0.5 volts

For Address Timing see Figure 5.

2 A new sample is obtained at every clock transition. Thus, the ϕ_1 and ϕ_2 clock frequencies are one-half the sampling frequency.

3 All logic signals normally swing between common and V_{dd}. Overdrive forwarded-biases diodes and must be avoided; underdrive may result in slow or faulty decoding.

CAPACITANCE OF INPUT LINES

TERMINAL	TYPICAL
ϕ_1 Clock Line	42pf
ϕ_2 Clock Line	42pf
Start	3pf
Signal Input Line	14pf
Strobe	37pf
Even Output	2pf
Odd Output	2pf
Each Address Line	21pf

Capacitances were measured on Boonton Model 72A capacitance meter with bias applied to the terminals of the device so as to obtain maximum capacitance reading within the specified operating range.